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43265
(52)

SEARCH REQUEST FORM

Examiner # (~~Mandatory~~): 76536 Requester's Full Name: Mano Padmanabhan

Art Unit 2671 Location (Bldg/Room#): PK2-6A39 Phone (circle 305 306 308) 2903

Serial Number: 09/283231 Results Format Preferred (circle): PAPER DISK E-MAIL

Title of Invention Image Processing Apparatus and Method of the same

Inventors (please provide full names): YOSHIKAZU KUROSE

Earliest Priority Date: 4/3/1998 (Japanese Priority info attached).

Keywords (include any known synonyms registry numbers, explanation of initialisms):

Synopsis: Basically, the system processes plurality of pixels simultaneously using plurality of pixel processors. Each pixel processor checks to see if the respective pixel is within the graphics primitive (polygon or triangle) it is processing. If it does not, then that processor could stop further processing, thus saving energy.

05-29-01 A09:16 IN

Search Topic:

Please write detailed statement of the search topic, and the concept of the invention. Describe as specifically as possible the subject matter to be searched. Define any terms that may have a special meaning. Give examples of relevant citations, authors, etc., if known. You may include a copy of the abstract and the broadcast or most relevant claim(s).

Image processing method/apparatus comprising:
- plurality of pixels processed simultaneously, preferably by plurality of circuits (claims 1, 21, 27)
- Z or depth comparison to determine pixel value to write (claim 21)
- use of flags & shift registers to control pipeline processing (claim 30)
- use of clock signal to activate/stop pixel processing circuits (claim 29)
- Texture blending based on α value / blending ratio / blending coefficient
- ~~Graphics~~ pipeline using a plurality of serially connected circuits.

STAFF USE ONLY

Searcher: E. Lytton
Searcher Phone #: 308-7793
Searcher Location: EIC 2600/2100
Date Picked Up: 6/8/01
Date Completed: 6/8/01
Clerical Prep Time: _____
Terminal Time: 115
Number of Databases: _____

Type of Search

_____	N.A. Sequence
_____	A.A. Sequence
_____	Structure (#)
✓	Bibliographic
_____	Litigation1
_____	Fulltext
_____	Procurement
_____	Other

Vendors (include cost where applicable)

_____	STN
_____	Questel/Orbit
_____	Lexis/Nexis
✓	WWW/Internet
_____	In-house sequence systems (list)
✓	Dialog
_____	Dr. Link
_____	Westlaw
_____	Other (specify)

B-18
FT-25

PTO-1590 (2-99)

COMMERCIAL DATABASE SEARCH FOR 09/283231

Prepared for: Mano Padmanabhan, 2671

By : Ellen Lytton, EIC2100/2600 308-7793

Date : June 8, 2001

Mano:

Attached is the search you requested on the processing of multiple pixels. Please let me know if you would like to refocus or modify the search in any way. Starting on 6/11 I will be back in EIC2100 and can be reached at 308-7793.

Ellen

File 350:Derwent WPIX 1963-2001/UD,UM &UP=200131
(c) 2001 Derwent Info Ltd
File 347:JAPIO OCT 1976-2001/Feb(UPDATED 010604)
(c) 2001 JPO & JAPIO
File 344:CHINESE PATENTS ABS APR 1985-2001/May
(c) 2001 EUROPEAN PATENT OFFICE

Set	Items	Description
S1	108539	PIXEL? OR PEL OR PELS OR SUBPIXEL? OR PICTURE()ELEMENT?
S2	8567	(PLURAL? OR MANY OR MULTI OR MULTIPLE OR MANY OR NUMEROUS - OR SEVERAL OR MORE(1W)ONE)(5W)S1
S3	65575	(SIMULTAN? OR SAME()TIME OR AT()ONCE OR TOGETHER OR PARALL-EL)(10N)(PROCESS??? OR PERFORM?(2N)OPERATION?)
S4	1122117	VALID? OR VALUE? ? OR S1(5N)(POLYGON? OR SHAPE? ? OR TRIAN-GLE? OR PRIMITIVE? OR GRAPHIC???(2W)UNIT? ?)
S5	128845	(CHECK? OR VERIF? OR MONITOR? OR CONFIRM? OR AUTHENTIC? OR JUDG? OR DETERMIN? OR EVALUAT?)(10N)S4
S6	7	S2 AND S3 AND S5
S7	259	AU=KUROSE Y?
S8	1	S7 AND S1
S9	188	S2 AND S3
S10	65654	FLAG? ? OR FLAGG? OR SHIFT(2W)REGISTER?
S11	9	S9 AND S10
S12	9	S11 NOT (S6 OR S8)
S13	4916	(CLOCK? ?(5N)SIGNAL????) AND (STOP? ? OR STOPP? OR HALT? OR TERMINAT? OR ABORT? OR DEACTIVAT? OR DE()ACTIVAT? OR CONTROL-?)(5N)(PROCESS??? OR OPERATION?)
S14	1	S9 AND S13
S15	1	S14 NOT (S6 OR S8 OR S12)
S16	86	S1 AND (S3 OR PIPELINE? OR PIPE()LINE? ?) AND S5
S17	3	S16 AND (S10 OR S13)
S18	3	S17 NOT (S11 OR S14 OR S6)

6/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012324601 **Image available**
WPI Acc No: 1999-130707/199911
XRPX Acc No: N99-095138

Images deconvolving apparatus for use in medical application apparatus such as MRI, PET and NMR apparatus - includes controller that reinitiates selector comparator and processor iteratively for subsequent iterations until highest intensity level in modified digitized image does not exceed predefined threshold

Patent Assignee: UNIV BOSTON (UYBO-N)
Inventor: COHEN N; VAN DE WETERING E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5862269	A	19990119	US 94346253	A	19941123	199911	B
			US 96624057	A	19960329		

Priority Applications (No Type Date): US 94346253 A 19941123; US 96624057 A 19960329
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5862269	A		32	G06K-009/54	Cont of application US 94346253

Abstract (Basic): US 5862269 A

NOVELTY - A processor (12) subtracts subtract image array from digitized image to generate a modified digitized image in response to comparison result. A controller reinitiates the selector, the comparator and processor for subsequent iterations until the highest intensity level in the modified digitized image does not exceed predefined threshold. A generator constructs the deconvolved digitized image from the modified digitized image. The display unit (22) displays the deconvolved digitized images. DETAILED DESCRIPTION - A digitization unit digitizes each image into image containing **several pixels** having specific intensity **values** . The pixel having highest intensity **value** is selected and is **determined** whether the selected pixel's highest intensity valve is above predefined threshold intensity in a comparator. Another generator generates subtract image array comprising subtract value for each peak feature of the digitized image only when the pixel with predefined threshold intensity. An INDEPENDENT CLAIM is also mentioned for describing method of deconvolving images.

USE - For use in medical application apparatus such as MRI, PET, NMR apparatus. For use with facsimile. For use in early foetus development using sonograms.

ADVANTAGE - Performs image **processing** at significantly improved **processing** speeds in **parallel processing** environment, since requirement of CLEAN method is eliminated. Performs deconvolution in real time application on standard hardware platform. Reduces number of iteration thereby significantly allowing dramatic reduction of subtractive stage and hence increases overall speed. DESCRIPTION OF DRAWING(S) - The figure depicts block diagram of imaging apparatus. (12) Processor; (22) Display unit.

Dwg.1/5

Title Terms: IMAGE; APPARATUS; MEDICAL; APPLY; APPARATUS; MRI; PET; NMR; APPARATUS; CONTROL; SELECT; COMPARATOR; PROCESSOR; ITERATIVE; SUBSEQUENT; ITERATIVE; HIGH; INTENSITY; LEVEL; MODIFIED; IMAGE; PREDEFINED; THRESHOLD
Derwent Class: S05; T01
International Patent Class (Main): G06K-009/54
International Patent Class (Additional): G06K-009/40
File Segment: EPI

6/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011385256 **Image available**
WPI Acc No: 1997-363163/199733
Related WPI Acc No: 1996-010321
XRPX Acc No: N97-301975

Pixel interpolation system for video processing - uses specified current interpolation weight for interpolating two input pixels and changes weighting factor incrementally for further sequential interpolation

Patent Assignee: INTEL CORP (ITLC)
Inventor: SPRAGUE D L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5646696	A	19970708	US 92995288	A	19921223	199733	B
			US 94267846	A	19940629		
			US 95461547	A	19950605		
			US 96654020	A	19960528		

Priority Applications (No Type Date): US 92995288 A 19921223; US 94267846 A 19940629; US 95461547 A 19950605; US 96654020 A 19960528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5646696	A		11		Cont of application US 92995288
					Cont of application US 94267846
					Cont of application US 95461547

Abstract (Basic): US 5646696 A

The system receives an input pixel stream via first and second line buffers (112,114). The first line buffer is coupled at its input to the input pixel stream and the second line buffer is coupled at its input to the first line buffer output. The buffers provide pixel pairs that are delayed by one scan line with the pixel pairs comprising vertically adjacent pixels. A vertical one-dimensional interpolator (122) receives the pixel pairs and a first sequence of interpolation weights which are provided by a vertical interpolation weight register (116). A interpolated **value** is **determined** between the vertically adjacent inputs.

A delay latch (126) delays one pixel of two consecutive vertically-interpolated pixels and provides pairs of horizontally adjacent, vertically-interpolated pixels. A horizontal one-dimensional interpolator (128) receives the of vertically-interpolated pixel pairs and a second sequence of interpolation weights which are provided by a horizontal interpolation weight register (130). The interpolator provides **several** vertically-interpolated **pixels** comprising sequential weighted sums of pixel pairs in accordance with the second sequence of interpolation weights. The delay latch is coupled at its input to the output of the vertical interpolator and to a first input of the horizontal interpolator and at its output to a second input of the horizontal interpolator.

ADVANTAGE - Uniform scaling of images. Interpolating **operation** can be **performed simultaneously** , vertically and horizontally.

Dwg.3/5

Title Terms: PIXEL; INTERPOLATION; SYSTEM; VIDEO; PROCESS; SPECIFIED; CURRENT; INTERPOLATION; WEIGHT; INTERPOLATION; TWO; INPUT; PIXEL; CHANGE; WEIGHT; FACTOR; INCREMENT; SEQUENCE; INTERPOLATION
Index Terms/Additional Words: VRAM
Derwent Class: T01; W04
International Patent Class (Main): H04N-009/74
File Segment: EPI

6/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010044233 **Image available**
WPI Acc No: 1994-311944/199439

XRPX Acc No: N94-245571

Offset determination between images of integrated circuit from charged particle beam appts. and CAD - using parallel processing **techniques by convolving pixels with Laplacian and Gaussian kernels, and correlating resulting images to identify maximum**

Patent Assignee: SCHLUMBERGER TECHNOLOGIES INC (SLMB)

Inventor: BARNARD R D

Number of Countries: 007 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 619551	A2	19941012	EP 94200568	A	19940307	199439	B
JP 7006230	A	19950110	JP 9444303	A	19940315	199511	
EP 619551	A3	19950816	EP 94200568	A	19940307	199613	
US 5604819	A	19970218	US 9331547	A	19930315	199713	
EP 619551	B1	20000112	EP 94200568	A	19940307	200008	
DE 69422539	E	20000217	DE 622539	A	19940307	200016	
			EP 94200568	A	19940307		

Priority Applications (No Type Date): US 9331547 A 19930315

Cited Patents: No-SR.Pub; 2.Jnl.Ref; EP 254643; EP 381067

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 619551	A2	E	39	G06F-015/70	
Designated States (Regional): DE FR GB IT NL					
EP 619551	B1	E		G06T-005/20	
Designated States (Regional): DE FR GB IT NL					
DE 69422539	E			G06T-005/20	Based on patent EP 619551
JP 7006230	A		27	G06T-007/00	
US 5604819	A		57	G06K-009/00	
EP 619551	A3			G06F-015/70	

Abstract (Basic): EP 619551 A

Two images are stored as pixel data in an X,Y grid with intensity values. For each image, a set of data describing each patch is retrieved from the pixel data for the images. The values are convolved with a zero-mean Laplacian kernel to produce Laplacian patches and further convolved with a Gaussian kernel to prepare registration images. Binarised images are produced by converting intensity values of pixels of the registration images.

The binarised images are bit-packed and correlated to one another by performing an exclusive-OR operation for each pixel location at a number of relative offsets of the images. The results of the exclusive-OR operation are summed to produce an image-correlation value for each relative offset, the highest value defining relative offset of the images.

USE/ADVANTAGE - In charged-particle beam systems to verify, characterise, design, debug and modify integrated circuits, e.g. electron beam to acquire waveforms on internal nodes and produce voltage-contrast images, focused ion beam for etching, milling, cutting metal lines, drilling holes, and depositing material to form metal connectors and pads, and scanning ion microscopes. Provides automatic control. Enables identification of image section against part of another.

Dwg.27/29

Title Terms: OFFSET; DETERMINE; IMAGE; INTEGRATE; CIRCUIT; CHARGE; PARTICLE ; BEAM; APPARATUS; CAD; PARALLEL; PROCESS; TECHNIQUE; PIXEL; LAPLACE; GAUSS; KERNEL; CORRELATE; RESULT; IMAGE; IDENTIFY; MAXIMUM

Derwent Class: T01; U11; V05

International Patent Class (Main): G06F-015/70; G06K-009/00; G06T-005/20; G06T-007/00

International Patent Class (Additional): H01L-021/66

File Segment: EPI

6/5/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

008806243 **Image available**
WPI Acc No: 1991-310255/199142
XRPX Acc No: N91-237867
Fingerprint correlation system with parallel **FIFO** processor - **scans** multi- pixel **reference, and image data relatively via FIFO buffers for comparison using XOR circuitry**
Patent Assignee: KNIGHT A W (KNIG-I)
Inventor: KNIGHT A W; KNIGHT D C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5054090	A	19911001	US 90555173	A	19900720	199142	B

Priority Applications (No Type Date): US 90555173 A 19900720

Abstract (Basic): US 5054090 A
The apparatus **parallel processes** ''live'' and pre-recorded ''reference'' fingerprint data for comparison purposes. An array sensor images a selected portion of a live fingerprint and video devices produce corresponding digital live image data. The pre-recorded, **multi -pixel** reference data and the image data are scanned relative to one another via recirculating First-in-First-Out (FIFO) buffer memories and row and column shift devices.
Exclusive OR (XOR), summation and accumulation circuitry simultaneously compare the reference and image data over a number of correlation cycles and compute a correlation **value** for each correlation cycle. A microprocessor **determines** the best correlation **value** of the reference and image data from a tabular store of correlation values for each correlation cycle relative to a PASS/FAIL threshold.
USE/ADVANTAGE - Credit card validation, personnel access control and computer security. Improved matching accuracy. (13pp Dwg.No.4A/6
Title Terms: FINGERPRINT; CORRELATE; SYSTEM; PARALLEL; FIFO; PROCESSOR; SCAN; MULTI; PIXEL; REFERENCE; IMAGE; DATA; RELATIVELY; FIFO; BUFFER; COMPARE; EXCLUSIVE-OR; CIRCUIT
Index Terms/Additional Words: FIRST; FIRST; CREDIT; CARD; VALID; ACCESS; SECURE
Derwent Class: S05; T04
International Patent Class (Additional): G06K-009/68
File Segment: EPI

6/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007615938
WPI Acc No: 1988-249870/198835
XRPX Acc No: N88-190309
Image understanding machine using elements with gated connections - stores each pixel of loaded image in memory of each processing element receiving unique label
Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: SHU B D; SHU D B
Number of Countries: 013 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8806322	A	19880825	WO 87US3301	A	19871214	198835	B
EP 301086	A	19890201				198905	
US 4809346	A	19890228	US 8713481	A	19870211	198911	
JP 1502220	W	19890803	JP 8713481	A	19870211	198937	
ES 2006312	A	19890416	ES 88368	A	19880210	198942	
IL 84933	A	19920525	IL 84933	A	19871223	199225	
EP 301086	B1	19921111	WO 87US3301	A	19871214	199246	
			EP 88902350	A	19871214		
DE 3782653	G	19921217	DE 3782653	A	19871214	199252	

WO 87US3301	A	19871214	
EP 88902350	A	19871214	

Priority Applications (No Type Date): US 8713481 A 19870211; US 86887847 A 19860718
Cited Patents: EP 121686; EP 203728; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8806322	A	E	72		
Designated States (National): JP					
Designated States (Regional): BE CH DE FR GB IT NL SE					
EP 301086	A	E			
Designated States (Regional): BE CH DE FR GB IT LI NL SE					
US 4809346	A		35		
EP 301086	B1	E	49	G06F-015/66	Based on patent WO 8806322
Designated States (Regional): BE CH DE FR GB IT LI NL SE					
DE 3782653	G			G06F-015/66	Based on patent EP 301086
					Based on patent WO 8806322
IL 84933	A			G06F-015/80	

Abstract (Basic): WO 8806322 A

The machine has a network of practically identical processing elements with a memory capable of storing a pixel value. A gate between each processing element and its neighbouring processing elements is adapted to connect each element to its neighbouring ones selectively. A control opens and closes the gates.

The control can close the gate between neighbouring processing elements when the pixel values stored in them are the same, the control opening the gate when the pixel values are different. Some/none logic can be used with input registers for each processing element able to receive test signals and output S/N lines for supplying a result associated with the test signal to each processing element.

USE/ADVANTAGE - Computer architectures capable of both arithmetic or iconic and symbolic processing of image data. Applies unique region labels faster. Besides region labelling gating connections can perform other functions, e.g. finding min. spanning tree, min., cost path, performing Hough transform and Boolean matrix multiplication.

Title Terms: IMAGE; UNDERSTAND; MACHINE; ELEMENT; GATE; CONNECT; STORAGE; PIXEL; LOAD; IMAGE; MEMORY; PROCESS; ELEMENT; RECEIVE; UNIQUE; LABEL
Index Terms/Additional Words: COMPUTER; VISION; ARCHITECTURE; SYMBOL; TRANSFORM
Derwent Class: T01; T04
International Patent Class (Main): G06F-015/66; G06F-015/80
International Patent Class (Additional): G06K-009/00
File Segment: EPI

6/5/6 (Item 6 from file: 350)

007402597 **Image available**
WPI Acc No: 1988-036532/198805
XRPX Acc No: N88-027599

Computer vision architecture e.g. for aircraft navigation - transforms image to symbolic form, provides high level description of image and attributes, and relationships to other objects in image

Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: NASH G J; SHU B D; NASH J G; SHU D B
Number of Countries: 011 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8800737	A	19880128	WO 87US1332	A	19870605	198805	B
EP 276237	A	19880803	EP 87904174	A	19870605	198831	
US 4809347	A	19890228	US 86887847	A	19860718	198911	
JP 1500780	W	19890316	JP 87503802	A	19870605	198917	
ES 2004645	A	19890116	ES 872097	A	19870717	198936	

IL 82826	A	19901223				199107
EP 276237	B1	19920722	EP 87904174	A	19870605	199230
			WO 87US1332	A	19870605	
DE 3780615	G	19920827	DE 3780615	A	19870605	199236
			EP 87904174	A	19870605	
			WO 87US1332	A	19870605	

Priority Applications (No Type Date): US 86887847 A 19860718
Cited Patents: 2.Jnl.Ref
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8800737	A	E	55		
Designated States (National): JP					
Designated States (Regional): BE DE FR GB IT NL SE					
EP 276237	A	E			
Designated States (Regional): BE DE FR GB IT NL SE					
US 4809347	A		27		
EP 276237	B1	E	37	G06F-015/62	Based on patent WO 8800737
Designated States (Regional): BE DE FR GB IT NL SE					
DE 3780615	G			G06F-015/62	Based on patent EP 276237
					Based on patent WO 8800737

Abstract (Basic): WO 8800737 A

The architectured understanding machine has one level (12) of image processing elements for operating on an image matrix on a pixel per processing element basis. The first level processing elements are adapted to communicate with each other. A second level (14) of processing elements operate on **several pixels** associated with a given array of first level processing elements. Each element is associated with a group of first level processing elements, providing communication between.

A third level (16) of processing elements, instructs the first and second level processing elements, as well as operating on a larger segment of the matrix than the second level processing elements. A host computer communicates with at least each third level processing element.

USE/ADVANTAGE - Development system in vision laboratory. High speed information transfer

Title Terms: COMPUTER; VISION; ARCHITECTURE; AIRCRAFT; NAVIGATION; TRANSFORM; IMAGE; SYMBOL; FORM; HIGH; LEVEL; DESCRIBE; IMAGE; ATTRIBUTE; RELATED; OBJECT; IMAGE
Derwent Class: T01; T04
International Patent Class (Main): G06F-015/62
International Patent Class (Additional): G06K-009/00
File Segment: EPI

6/5/7 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

00803206 **Image available**
DETECTING METHOD OF FOCUSSING

PUB. NO.: 56-123506 [JP 56123506 A]
PUBLISHED: September 28, 1981 (19810928)
INVENTOR(s): SUZUKI TAKEOMI
AOKI MASAHIRO
OIKAMI KENICHI
IDA MASATOSHI
APPLICANT(s): OLYMPUS OPTICAL CO LTD [000037] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-026727 [JP 8026727]
FILED: March 05, 1980 (19800305)
INTL CLASS: [3] G02B-007/11; G03B-003/00
JAPIO CLASS: 29.2 (PRECISION INSTRUMENTS -- Optical Equipment); 29.1 (PRECISION INSTRUMENTS -- Photography & Cinematography)

JOURNAL: Section: P, Section No. 94, Vol. 05, No. 201, Pg. 162, December 19, 1981 (19811219)

ABSTRACT

PURPOSE: To simplify the constitution and to enable the detection of focus quickly and with high accuracy, by comparing parallelly between the D/A conversion value of a digital output of CPU and a **plurality** of **picture element** information and deciding the A/D conversion range and digitizing the picture element information.

CONSTITUTION: Digital **values** LH, L(sub 1), L(sub 2), LL **determining** the range of A/D conversion such as 3 stages A-C, with CPU5, are sequentially converted into analog values at a D/A converter 20, and the ranges A-C corresponding to the picture element information are decided via the OR circuit 23, through the parallel comparison with the picture element information in sample-hold at capacitors 18(sub 1)... through the detection of the photodetecting array 3A corresponding to the picture elements with comparators 19(sub 1).... Then, the CPU5 transmits the digital reference signal sequentially changed in the determined ranges A-C, and with the same processing, picture element information can surely be digitized with quick **processing** even with weak contrast by a simple constitution in **parallel** comparison by an AND circuit 23, digital memory 21(sub 1)..., and decoder 24. Thus, the detection of focus can quickly be made with high accuracy.
?

8/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012767617 **Image available**
WPI Acc No: 1999-573737/199949
XRPX Acc No: N99-423058

Computer graphics image processor

Patent Assignee: SONY CORP (SONY)
Inventor: **KUROSE Y**
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 947978	A2	19991006	EP 99400838	A	19990406	199949	B
JP 11345218	A	19991214	JP 9951795	A	19990226	200009	
CA 2268210	A1	19991003	CA 2268210	A	19990401	200010	
KR 99082898	A	19991125	KR 9911650	A	19990402	200055	

Priority Applications (No Type Date): JP 9951795 A 19990226; JP 9891844 A 19980403
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 947978	A2	E	30	G09G-005/00	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
JP 11345218	A		25	G06F-015/16	
CA 2268210	A1	E		G06T-001/00	
KR 99082898	A			G06T-001/20	

Abstract (Basic): EP 947978 A2

NOVELTY - Processor comprises **pixel** processing circuits with a controller using a clock signal. The controller stops the clock signal when **pixel** processing is not required. A texture engine circuit (12) calculates data coordinates using a texture buffer with z comparison and blending using memory I/F circuit (13) in a pipeline system of operation blocks (200-205).

DETAILED DESCRIPTION - There is an INDEPENDENT CLAIM for an image processing method fir performing image processing by using **pixel** processing circuits, and an image processing method for expressing an image to be displayed on a display.

USE - Processor is for use in CAD applications and amusement machine computer graphics.

ADVANTAGE - Processor has reduced power consumption.

DESCRIPTION OF DRAWING(S) - The figure shows the texture engine circuit and memory I/F circuit.

pp; 30 DwgNo 3/12

Title Terms: COMPUTER; GRAPHIC; IMAGE; PROCESSOR
Derwent Class: P85; T01
International Patent Class (Main): G06F-015/16; G06T-001/00; G06T-001/20; G09G-005/00
International Patent Class (Additional): G06T-015/00
File Segment: EPI; EngPI

12/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011937426 **Image available**
WPI Acc No: 1998-354336/199831
XRPX Acc No: N98-277462
Decoder for image data encoded by predictive encoding system adopting JBIG - has multiplexer which chooses either of reverse predictor and state value from RAM, based on decoding result output from arithmetic decoding unit
Patent Assignee: FUJI XEROX CO LTD (XERF)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10136212	A	19980522	JP 96288731	A	19961030	199831	B
JP 3141794	B2	20010305	JP 96288731	A	19961030	200115	

Priority Applications (No Type Date): JP 96288731 A 19961030
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10136212	A		13	H04N-001/417	
JP 3141794	B2		12	H04N-001/417	Previous Publ. patent JP 10136212

Abstract (Basic): JP 10136212 A
The decoder chooses a reference pixel from **several pixels** positioned on the periphery of an attention pixel. A RAM (33) which includes two lead ports, is provided. Condition of reference pixel is output by a **shift register** (32). Maximum and minimum values (1,0) which are accessed by the pixel during decoding is into the lead ports. A probability estimation table (6) is provided which passes LSZ to a arithmetic decoding unit (21) based on the state value.
The arithmetic decoding unit performs decoding process of code series based on LSZ and the reverse predictor. A multiplexer (35) chooses either of reverse predictor (23) and state value (5) from the RAM, based on the decoding result output from the arithmetic decoding unit.
ADVANTAGE - Performs predictive coding at high speed. Performs read-out and decoding **process simultaneously** . Shortens decoding time.
Dwg.1/16
Title Terms: DECODE; IMAGE; DATA; ENCODE; PREDICT; ENCODE; SYSTEM; ADOPT; MULTIPLEX; CHOICE; REVERSE; PREDICT; STATE; VALUE; RAM; BASED; DECODE; RESULT; OUTPUT; ARITHMETIC; DECODE; UNIT
Derwent Class: U21; W02
International Patent Class (Main): H04N-001/417
International Patent Class (Additional): H03M-007/36; H04N-007/32
File Segment: EPI

12/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011518403 **Image available**
WPI Acc No: 1997-494889/199746
XRPX Acc No: N97-412053
Parallel processing **type image** processor - **has recognition unit which determines array pattern set of specific pattern based on computed distance between area of image data from distance calculator**
Patent Assignee: CANON KK (CANO)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9231356	A	19970905	JP 9633622	A	19960221	199746	B

Priority Applications (No Type Date): JP 9633622 A 19960221
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 9231356 A 21 G06T-007/00

Abstract (Basic): JP 9231356 A
The processor recognises whether an image data contains a specific pattern. **Several pixel** lines of a predetermined length are contained in the image data. An image input unit (102) inputs each pixel line to an **operation** unit which **performs** a **parallel processing** to obtain the specific pattern. A distinction unit detects the obtained specific pattern.

A coordinate calculator computes the coordinate position in the predetermined area of the image data in accordance with the detected specific pattern. A distance calculator computes a distance between the area based on the computed coordinate position. A recognition unit determines the array pattern set of the specific pattern based on the computed distance between the area.

ADVANTAGE - Offers high-speed image **processing** by using switching of **flag** and **operation** mode to **perform parallel processing** . Highly recognises specific pattern using pattern recognition unit. Offers high speed hardware processing for exclusive use by providing software to perform flexible process.

Dwg.1/54
Title Terms: PARALLEL; PROCESS; TYPE; IMAGE; PROCESSOR; RECOGNISE; UNIT; DETERMINE; ARRAY; PATTERN; SET; SPECIFIC; PATTERN; BASED; COMPUTATION; DISTANCE; AREA; IMAGE; DATA; DISTANCE; CALCULATE
Derwent Class: T01
International Patent Class (Main): G06T-007/00
File Segment: EPI

12/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010536304 **Image available**
WPI Acc No: 1996-033258/199604
XRPX Acc No: N96-028070
Parallel processing **type signal** processing **device - has** shift register **which performs number of data transfers between processors**
Patent Assignee: TOSHIBA AVE KK (TOSA); TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 7271745 A 19951020 JP 9459151 A 19940329 199604 B

Priority Applications (No Type Date): JP 9459151 A 19940329
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 7271745 A 7 G06F-015/173

Abstract (Basic): JP 7271745 A
The signal processing device consists of a number of processors which perform calculations or operations on an input data based on the increments of counts in the program counter. A number of processors and a number of registers are connected annularly. This set up is used for data transmission. A **shift register** performs data shifting operation between processors after every clock signal of a very high frequency.

USE/ADVANTAGE - In e.g. image signal processing. Raises data communication speed between processors. Realizes pixel shift processing of **many** stages such as rearrangement of **pixel** data in short time.

Dwg.1/7
Title Terms: PARALLEL; PROCESS; TYPE; SIGNAL; PROCESS; DEVICE; SHIFT; REGISTER; PERFORMANCE; NUMBER; DATA; TRANSFER; PROCESSOR
Derwent Class: T01

International Patent Class (Main): G06F-015/173
International Patent Class (Additional): G06F-015/163; G06T-001/20
File Segment: EPI

12/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010219853 **Image available**
WPI Acc No: 1995-121108/199516
XRPX Acc No: N95-095600
Image signal encoder and decoder - writes several pixel **data arranged in** parallel **form into memory unit and** processes **them to isolate luminance and chrominance components along every horizontal line**
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: ISHIWATA S
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7046628	A	19950214	JP 93158531	A	19930629	199516	B
US 5541658	A	19960730	US 94265929	A	19940627	199636	

Priority Applications (No Type Date): JP 93158531 A 19930629
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7046628	A		7	H04N-011/04	
US 5541658	A		21	H04N-007/12	

Abstract (Basic): JP 7046628 A

The encoder-decoder accesses **several** digital colour image signal **processing pixel** data arranged in **parallel** and stored in a memory apparatus (3). An image signal encoder compresses and encodes this pixel data.

When pixel data in a field is processed, luminance and chrominance components of the pixel data are isolated. The isolated pixel data of one horizontal line is not allowed to spread to more than two horizontal lines along the perpendicular direction. An input output circuit (4) is provided to input and output data to the memory device.

ADVANTAGE - Increases amount of effective data which is to be written to memory in unit time when processing a field. Reduces memory reading and writing time and idle operational processing time. Reduces time taken to restore image of one field.

Dwg.1/4

Title Terms: IMAGE; SIGNAL; ENCODE; DECODE; WRITING; PIXEL; DATA; ARRANGE; PARALLEL; FORM; MEMORY; UNIT; PROCESS; ISOLATE; LUMINOUS; CHROMINANCE; COMPONENT; HORIZONTAL; LINE
Derwent Class: T01; W02; W04
International Patent Class (Main): H04N-007/12; H04N-011/04
International Patent Class (Additional): G06T-009/00; H04N-007/24; H04N-009/64
File Segment: EPI

12/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2001 Derwent Info Ltd. All rts. reserv.

004591893
WPI Acc No: 1986-095237/198615
XRPX Acc No: N86-069805
Peripheral appts. for image memory - has shift register **which holds display data of n pixels read out from RAM blocks in parallel**
Patent Assignee: HITACHI LTD (HITA)
Inventor: KATOH T; KOBAYASHI Y; TAKENAGA H
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 176801	A	19860409				198615	B
CA 1237529	A	19880531				198826	
US 4766431	A	19880823	US 85772695	A	19850905	198836	
KR 9005297	B	19900727				199133	
EP 176801	B1	19940209	EP 85111248	A	19850905	199406	
DE 3587750	G	19940324	DE 3587750	A	19850905	199413	
			EP 85111248	A	19850905		

Priority Applications (No Type Date): JP 84184658 A 19840905
Cited Patents: 2.Jnl.Ref; A3...8845; EP 106121; EP 106601; EP 147500; No-SR.Pub; WO 8202615
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 176801	A	E	43		
Designated States (Regional): DE FR GB					
EP 176801	B1	E	30	G09G-001/16	
Designated States (Regional): DE FR GB					
DE 3587750	G			G09G-001/16	Based on patent EP 176801

Abstract (Basic): EP 176801 A

The appts. includes a read data processing unit with a selector which receives image data of N pixels recd. out from n RAM blocks in parallel, selects the data of one of the pixels desagrated by a block address signal and sends out the selected data to an external processor. A write data processing unit receives the processed data, modifies this data in accordance with a function signal and writes the modified data into a memory assembly. The appts. also include a display data processing unit with a **shift register** which holds the display data of n pixles read out from the RAM blocks in parallel and a **shift register** which takes the content of the first **shift register** and outputs display data for each pixel.

A control unit supplies the modification function signal and an access mode signal fro the display data processing unit, in response to instruction from the external processor.

ADVANTAGE - Can be operated in nibble or page mode, allows feedback processing, allows modification between data already written and to be written afresh. (43pp Dwg No. 3/11

Title Terms: PERIPHERAL; APPARATUS; IMAGE; MEMORY; SHIFT; REGISTER; HOLD; DISPLAY; DATA; N; PIXEL; READ; RAM; BLOCK; PARALLEL
Index Terms/Additional Words: DYNAMIC
Derwent Class: P85; T04
International Patent Class (Main): G09G-001/16
International Patent Class (Additional): G06F-003/15; G06F-015/64
File Segment: EPI; EngPI

12/5/6 (Item 1 from file: 347)

04400485 **Image available**
Z BUFFER CONTROL CIRCUIT

PUB. NO.: 06-044385 [JP 6044385 A]
PUBLISHED: February 18, 1994 (19940218)
INVENTOR(s): MURATA MASAHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-197338 [JP 92197338]
FILED: July 24, 1992 (19920724)
INTL CLASS: [5] G06F-015/72; G06F-003/153
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JOURNAL: Section: P, Section No. 1743, Vol. 18, No. 278, Pg. 64, May 26, 1994 (19940526)

ABSTRACT

PURPOSE: To provide high-speed plotting by simultaneously calculating a Z value for **plural picture elements** at the time of plotting a horizontal line concerning the acceleration of Z buffer processing in the field of three-dimensional graphics.

CONSTITUTION: A three-dimensional image display device is provided with a frame memory 4 for simultaneously writing the **plural** horizontal **picture elements** and for permitting the write of the individually designated picture element among them, Z buffer memory 3 for simultaneously reading/writing **plural** values corresponding to thise **picture elements** and for permitting the write of the respectively designated picture element among them, plotting mode designation **flag** 27 to distinguish whether plotting is a horizontal line or a straight line at any arbitrary angle, and plural Z value arithmetic circuits 30 and when the plotting mode designation **flag** 27 designates the plotting of the horizontal line, the plural bits of the Z buffer memory 3 are **simultaneously processed** .

12/5/7 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

02674278 **Image available**
DIGITAL SIGNAL PROCESSOR

PUB. NO.: 63-291178 [JP 63291178 A]
PUBLISHED: November 29, 1988 (19881129)
INVENTOR(s): YAMADA HARUYASU
MORI TOSHIKI
AONO KUNITOSHI
MARUYAMA MASAKATSU
TOYOKURA MAKI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-126207 [JP 87126207]
FILED: May 22, 1987 (19870522)
INTL CLASS: [4] G06F-015/66
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS); R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS
JOURNAL: Section: P, Section No. 845, Vol. 13, No. 116, Pg. 130, March 22, 1989 (19890322)

ABSTRACT

PURPOSE: To execute a high speed picture **processing** by providing a function for **simultaneously** loading a program in **plural** memories and **processing** the respective **picture elements** of a picture signal in **parallel** .

CONSTITUTION: The titled processor is provided with a local picture **shift register** 2, the plural picture memories 4-1-4-4 for storing the contents of the **shift register** 2, plural arithmetic blocks 1-1-1-4 for processing the picture based on the data of the picture memories 4-1-4-4, plural program memories and controllers 5-1-5-4 for controlling the arithmetic blocks 1-1-1-4 and the function for simultaneously loading the program in the plural program memories 5-1-5-4. The respective picture elements of the picture signal are **processed** in **parallel** . Since this is the **parallel processing** for every picture element of the picture signal, a higher instruction such as a condition jump instruction or the like can be executed in a next instruction cycle without a waiting time. Thereby, a more complicate picture processing can be realized at high speed and a real time processing is easily executed.

12/5/8 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

01482070 **Image available**
BINARY PICTURE DECODER

PUB. NO.: 59-193670 [JP 59193670 A]
PUBLISHED: November 02, 1984 (19841102)
INVENTOR(s): TANABE NAOTO
UENO YUTAKA
SEMASA TAKAYOSHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-067380 [JP 8367380]
FILED: April 15, 1983 (19830415)
INTL CLASS: [3] H04N-001/41
JAPIO CLASS: 44.7 (COMMUNICATION -- Facsimile)
JOURNAL: Section: E, Section No. 301, Vol. 09, No. 53, Pg. 111, March 07, 1985 (19850307)

ABSTRACT

PURPOSE: To improve the processing speed by separating the entire device into two devices for detecting a coding mode and for restoring a picture signal and absorbing the difference of the processing speed between both devices by means of an FIFO memory so as to execute two independent processings in parallel.

CONSTITUTION: A binary picture decoder consists of a coding mode detector 100 and a picture signal restoring device 200, a code word series inputted to a coding memory 5 of the device 100 is stored temporarily, a coding mode detecting circuit 6 detects the code by the control of the 1st control circuit 4a so as to decide the code word mode. The decided code word mode is stored tentatively in the FIFO memory 8 and read to a changing point detecting circuit 11 under the control of the 2nd control circuit 4b of the device 200. Further, a restored picture value comprising a signal of **plural picture elements** is stored in an FF7 sequentially by means of a line memory 1 and a **shift register** 10 or the like in response to the coding mode of the circuit 11, so as to execute the code mode detection and the picture signal restoration independently in **parallel** thereby quickening the **processing** speed.

12/5/9 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

01477868 **Image available**
PICTURE PROCESSING DEVICE

PUB. NO.: 59-189468 [JP 59189468 A]
PUBLISHED: October 27, 1984 (19841027)
INVENTOR(s): AONO KUNITOSHI
YAMADA HARUYASU
HASEGAWA KENICHI
MORI TOSHIKI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-063884 [JP 8363884]
FILED: April 12, 1983 (19830412)
INTL CLASS: [3] G06F-015/20; G09G-001/02
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 44.9 (COMMUNICATION -- Other)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS); R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS
JOURNAL: Section: P, Section No. 339, Vol. 09, No. 50, Pg. 162, March 05, 1985 (19850305)

ABSTRACT

. PURPOSE: To enable to process a digital picture processing such as smoothing, edge detection etc. at a high speed by containing **simultaneously** a picture element data whose signal is to be **processed** and eight nearby picture element data in a **shift register** .

CONSTITUTION: An input picture 31 is written successively in picture memories 33-35 divided into **plural** number, and **picture element** data of nearby point of picture data to be signal **processed** are read out in **parallel** from picture memories 33-35. The picture element data are inputted to a multiplexer 37 and rearranged, and inputted to **shift registers** 38-40. Data are read out in parallel from each step of **shift registers** 38-40 in synchronizing with scanning of the picture, and after processing in a signal processing circuit 41, the output picture 42 is outputted.

15/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05215863 **Image available**
DISPLAY DEVICE

PUB. NO.: 08-171363 [JP 8171363 A]
PUBLISHED: July 02, 1996 (19960702)
INVENTOR(s): NAKAJIMA YOSHIHARU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-280101 [JP 94280101]
FILED: October 19, 1994 (19941019)
INTL CLASS: [6] G09G-003/36; G02F-001/133; H04N-005/66
JAPIO CLASS: 44.9 (COMMUNICATION -- Other); 29.2 (PRECISION INSTRUMENTS -- Optical Equipment); 44.6 (COMMUNICATION -- Television)
JAPIO KEYWORD: R011 (LIQUID CRYSTALS)

ABSTRACT

PURPOSE: To prevent the occurrence of a vertical stripe ghost in a **plural pixels** simultaneous sampling system.

CONSTITUTION: A display panel 1 is provided with a horizontal drive circuit 13 simultaneously sampling a pixel 11 in a crossing part between gate and data lines X, Y orthogonal each other and plural video signals SIG1, 2, 3 and distributing them to data lines Y of the number of prescribed pieces. A video driver 2 delay processes plural video signals SIG1, 2, 3 according to the arrangement pitch of the pixel 11, and adjusts the supply timing of the video signals to the display panel 1. A timing generator 3 supplies a **clock signal** HCK to the horizontal drive circuit 13, and performs timing control of **simultaneous** sampling to **control** the delay **processing** of the video driver 2. Further, it optimizes the supply timing of the video signals SIG1, 2, 3 inputted to the display panel 1 for the timing of the simultaneous sampling.

18/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009925712 **Image available**
WPI Acc No: 1994-193423/199424
XRPX Acc No: N94-152259
Arithmetic processing e.g. addition, subtraction for image processing - performing arithmetic operation in parallel on composite operand contg. multi-bit data items to produce multi-bit result for each item, and obtaining flag bit by comparison of each component with value or range
Patent Assignee: XEROX CORP (XERO)
Inventor: DAVIES D
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 602887	A1	19940622	EP 93309862	A	19931208	199424	B
US 5375080	A	19941220	US 92993213	A	19921218	199505	
EP 602887	B1	20000315	EP 93309862	A	19931208	200018	
DE 69328071	E	20000420	DE 628071	A	19931208	200026	
			EP 93309862	A	19931208		

Priority Applications (No Type Date): US 92993213 A 19921218
Cited Patents: EP 464601; EP 486143
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 602887	A1	E	16	G06F-007/48	
Designated States (Regional): DE FR GB					
EP 602887	B1	E		G06F-007/48	
Designated States (Regional): DE FR GB					
DE 69328071	E			G06F-007/48	Based on patent EP 602887
US 5375080	A		17	G06F-007/00	

Abstract (Basic): EP 602887 A
The **processor performs** an arithmetic **operation** in **parallel** on a composite operand that includes several component data items (12, 14, 16), each having more than one bit. For each component item the operation produces a resulting data item, also having more than one bit.
For each component data item, a **flag** bit (32, 34, 36) indicates the result of a binary operation on the component. The binary operation compares a component data item with a threshold, or determines whether it is in a range, or compares it with a value for equality.
USE/ADVANTAGE - E.g. for document services - facsimile photocopier, printer, scanner of grey scale or colour images, searching image database, scanning envelopes for addresses, interpreting forms for high speed scanner, machine vision and process-specific print image correction and verification, **pixel** counting, grey-scale morphology, grey-scale rotation, generating error-diffused images and skew detection, finite difference analysis or simulation of physical phenomena. Technique permits efficient binary outcome operations in parallel on composite operands, which include several multi-bit component data items.
Dwg.1/9
Title Terms: ARITHMETIC; PROCESS; ADD; SUBTRACT; IMAGE; PROCESS; PERFORMANCE; ARITHMETIC; OPERATE; PARALLEL; COMPOSITE; OPERAND; CONTAIN; MULTI; BIT; DATA; ITEM; PRODUCE; MULTI; BIT; RESULT; ITEM; OBTAIN; **FLAG** ; BIT; COMPARE; COMPONENT; VALUE; RANGE
Derwent Class: S06; T01; T04; W02
International Patent Class (Main): G06F-007/00; G06F-007/48
International Patent Class (Additional): G06F-007/50
File Segment: EPI

18/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007457932 **Image available**
WPI Acc No: 1988-091866/198813
XRPX Acc No: N88-069375

Resolution extension of line or matrix imaging camera - using fringe grey scale digitisation with interpolation between pixels **on either side of video threshold level**

Patent Assignee: FRAUNHOFER-GES FORD ANGE (FRAU); PFEIFER T (PFEI-I)
Inventor: MOLITOR M
Number of Countries: 013 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8802097	A	19880324	WO 87DE423	A	19870918	198813	B
DE 3731531	A	19880407	DE 3731531	A	19870918	198815	
EP 324757	A	19890726	EP 87906154	A	19870918	198930	
JP 2500684	W	19900308	JP 87505591	A	19870918	199016	
DE 3731531	C	19900523				199021	
EP 324757	B	19911211				199150	
DE 3775218	G	19920123				199205	

Priority Applications (No Type Date): DE 3632070 A 19860920
Cited Patents: No-SR.Pub; FR 2512945; GB 2058344; JP 59099304; US 4650335
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8802097	A	G	38		
Designated States (National): JP US					
Designated States (Regional): AT BE CH DE FR GB IT LU NL SE					
EP 324757	A	G			
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					
EP 324757	B				
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					

Abstract (Basic): WO 8802097 A

Analogue signals from a semiconductor camera (9) are converted (10) into binary values of dual word length (k) from which all but the most significant bit of the absolute value representing **pixel** distance from a 50 percent threshold level are **processed** in two **parallel shift registers** (11).

The read-out clock data word is stored in a latch register (12) for further calculation using an EPROM (13) and edge detector (14). By interpolation between two **pixels** of a fringe transition, one above and one below the threshold, the dark/light distribution or the fringe position is expressible with greater resolution than the spatial frequency of the imager.

USE/ADVANTAGE - Measuring length in micrometre range. Spatial resolution is enhanced without detriment to read-out speed. Any desired number of fringes can be included and measured.

5/10

Title Terms: RESOLUTION; EXTEND; LINE; MATRIX; IMAGE; CAMERA; FRINGE; GREY; SCALE; DIGITAL; INTERPOLATION; **PIXEL** ; SIDE; VIDEO; THRESHOLD; LEVEL
Index Terms/Additional Words: FINE; LENGTH; MEASURE
Derwent Class: S02; T04; W04
International Patent Class (Additional): G01B-011/02
File Segment: EPI

18/5/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03185063 **Image available**
IMAGE DATA CORRECTION SYSTEM

PUB. NO.: 02-160563 [JP 2160563 A]
PUBLISHED: June 20, 1990 (19900620)
INVENTOR(s): MINOWA NOBUYUKI

HIRASAWA AKIHISA
OKUYAMA MAKOTO
TAKAHASHI TSUGIO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-313863 [JP 88313863]
FILED: December 14, 1988 (19881214)
INTL CLASS: [5] B41J-002/44; H04N-001/04; H04N-001/23
JAPIO CLASS: 29.4 (PRECISION INSTRUMENTS -- Business Machines); 44.7 (COMMUNICATION -- Facsimile)
JAPIO KEYWORD: R002 (LASERS)
JOURNAL: Section: M, Section No. 1021, Vol. 14, No. 416, Pg. 86, September 07, 1990 (19900907)

ABSTRACT

PURPOSE: To permit **pixel** data to be controlled as logic **value** and thereby obtain correct density gradation by **determining** the linkage between black and white data of **pixel** data and then controlling the laser beam projection time at the head or rear end of a laser beam control clock.

CONSTITUTION: Image data received from an external device 1 is synchronized by dot by means of a clock from an oscillation circuit 9, and then is latched by a latching circuit 2. **Pixel** data which is output from the latching circuit 2 is entered in a **shift register** 11. A single dot **pixel** data A is divided into four portions by means of a clock C from an oscillation circuit 10, and when eight dots of data (8 dots by dither **processing**) are latched, 32 bits of data are output in **parallel** from the **shift register** 11 as an address in the ROM 12 to identify the data and output the corrected **pixel** data B. The corrected **pixel** data B of **pixel** data A is output as data short by 1/4 of the hour before and after the **pixel** data A, if the dot is identified as an independent black dot 1. Then a laser driver 3 is driven to permit a semiconductor laser 4 to emit light. This process is performed sequentially as described in the above action up to the output of the corrected **pixel** data B.

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File   2:INSPEC 1969-2001/Jun W1
         (c) 2001 Institution of Electrical Engineers
File   8:Ei Compendex(R) 1970-2001/Jun W1
         (c) 2001 Engineering Info. Inc.
File   6:NTIS 1964-2001/Jun W4
         Comp&distr  2000 NTIS, Intl Cpyrght All Right
File  99:Wilson Appl. Sci & Tech Abs 1983-2001/Apr
         (c) 2001 The HW Wilson Co.
File 144:Pascal 1973-2001/Jun W1
         (c) 2001 INIST/CNRS
File  77:Conference Papers Index 1973-2001/May
         (c) 2001 Cambridge Sci Abs
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         (c) 2001 Pira International

Set     Items   Description
S1     103029   PIXEL? OR PEL OR PELS OR SUBPIXEL? OR PICTURE()ELEMENT?
S2       1878   (PLURAL? OR MANY OR MULTI OR MULTIPLE OR MANY OR NUMEROUS -
            OR SEVERAL OR MORE(1W)ONE)(5W)S1
S3     176955   (SIMULTAN? OR SAME()TIME OR AT()ONCE OR TOGETHER OR PARALL-
            EL)(5N)(PROCESS??? OR PERFORM?(2N)OPERATION?)
S4    3524592   VALID? OR VALUE? ? OR S1(5N)(POLYGON? OR SHAPE? ? OR TRIAN-
            GLE? OR PRIMITIVE? OR GRAPHIC???(2W)UNIT? ?)
S5     243914   (CHECK? OR VERIF? OR MONITOR? OR CONFIRM? OR AUTHENTIC? OR
            JUDG? OR DETERMIN? OR EVALUAT?)(5N)S4
S6          0   S2 AND S3 AND S5
S7         24   S1 AND S3 AND S5
S8         18   S7 NOT PY,CY=1999:2001
S9         16   RD (unique items)
S10     26556   FLAG? ? OR FLAGG? OR SHIFT(2W)REGISTER?
S11         3   S2 AND S3 AND S10
S12         3   S11 NOT S7
S13         3   RD (unique items)
S14       129   (CLOCK? ?(5N)SIGNAL????) AND (STOP? ? OR STOPP? OR HALT? OR
             TERMINAT? OR ABORT? OR DEACTIVAT? OR DE()ACTIVAT? OR CONTROL-
            ?)(5N)(PROCESS??? OR OPERATION?)
S15         0   S2 AND S3 AND S14
S16       345   AU=(KUROSE, Y? OR KUROSE Y?)
S17         0   S16 AND S1
S18         6   S16 AND IMAGE?(5N)PROCESS?
S19         6   RD (unique items)
```

9/5/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6331573 INSPEC Abstract Number: B1999-10-6135-058, C1999-10-5260B-075
Title: An information-theoretical approach to saliency maps construction
Author(s): Battiato, S.; Gallo, G.
Author Affiliation: Dipt. di Matematica, Catania Univ., Italy
Conference Title: 6th European Congress on Intelligent Techniques and Soft Computing. EUFIT '98 Part vol.2 p.1375-9 vol.2
Publisher: Verlag Mainz, Aachen, Germany
Publication Date: 1998 Country of Publication: Germany 3 vol. xxvi+2010 pp.
ISBN: 3 89653 500 5 Material Identity Number: XX-1999-02104
Conference Title: 6th European Congress on Intelligent Techniques and Soft Computing. EUFIT '98
Conference Date: 7-10 Sept. 1998 Conference Location: Aachen, Germany
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T); Experimental (X)
Abstract: In this paper a new image space approach to learn the most relevant (in an information-theoretic sense) mixture of measured characteristic of a **pixel** to **determine** a saliency **value** is proposed and discussed. The methods tries to bring **together** entropy-based image **processing** methods, statistics smoothing of irregular and sparse data and principal components analysis techniques. Some applications and examples are also discussed. (8 Refs)
Subfile: B C
Descriptors: computer vision; entropy; information theory; principal component analysis; smoothing methods
Identifiers: information-theory; saliency maps construction; image space; entropy; image processing; statistics smoothing; principal components analysis; computer vision
Class Codes: B6135 (Optical, image and video signal processing); B6110 (Information theory); B0240Z (Other topics in statistics); C5260B (Computer vision and image processing techniques); C1260 (Information theory); C1140Z (Other topics in statistics)

9/5/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5164403 INSPEC Abstract Number: B9603-6140C-071, C9603-1250-033
Title: Orthogonal-function-based image filtering and edge detection
Author(s): Jun Shen; Wei Shen; Dan-Fei Shen
Author Affiliation: Inst. of Geodynamics, Bordeaux-3 Univ., Talence, France
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2620 p.703-10
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1995 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1995)2620L.703:OFBI;1-4
Material Identity Number: C574-95238
U.S. Copyright Clearance Center Code: 0 8194 2012 3/95/$6.00
Conference Title: International Conference on Intelligent Manufacturing
Conference Sponsor: Nat. Natural Sci. Found.; Huazhong Univ. Sci. & Technol.; SPIE; K.C. Wong Educ. Found
Conference Date: 14-17 June 1995 Conference Location: Wuhan, China
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: Filtering and edge detection are widely used in image processing and computer vision. The following problems are important:

computational complexity; precision; the potential for parallel realization; and **subpixel** precision edge detection. Using orthogonal polynomial theory we propose a new development of image filters and their derivatives for edge detection, which has a reduced and constant complexity and good precision. In particular, we present Hermite integration for Gaussian filters and Laguerre integration for Shen-Castan filters. We show that the output of these filters can be calculated by the weighted sum of the signal **values** at positions **determined** by the roots of orthogonal polynomials. Generalization to M-D cases and to derivative calculation for edge detection, and the implementation in discrete cases are also presented. Our method has been implemented and tested for computer-generated and real images, and the experimental results were satisfactory. (25 Refs)

Subfile: B C

Descriptors: computational complexity; computer vision; digital filters; edge detection; filtering theory; image processing

Identifiers: orthogonal-function-based image filtering; edge detection; image processing; computer vision; computational complexity; **subpixel** precision; **parallel processing** ; orthogonal polynomial theory; Hermite integration; Gaussian filters; Laguerre integration; Shen-Castan filters; real images

Class Codes: B6140C (Optical information, image and video signal processing); C1250 (Pattern recognition); C1260 (Information theory); C5260B (Computer vision and image processing techniques); C5240 (Digital filters)

9/5/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

4846404 INSPEC Abstract Number: C9502-6130B-010

Title: Load balancing strategies for ray tracing on parallel processors

Author(s): Tong-Yee Lee; Raghavendra, C.S.; Nicholas, J.B.

Author Affiliation: Sch. of EE, Washington State Univ., Pullman, WA, USA

Part vol.1 p.177-81 vol.1

Editor(s): Chan, T.K.

Publisher: IEEE, New York, NY, USA

Publication Date: 1994 Country of Publication: USA 2 vol. xxvii+1111 pp.

ISBN: 0 7803 1862 5

Conference Title: Proceedings of TENCON'94 - 1994 IEEE Region 10's 9th Annual International Conference on: 'Frontiers of Computer Technology'

Conference Sponsor: IEEE Region 10; Comput. Chapter, IEEE Singapore Sect. ; Inst. Eng., Singapore; IEEE Comput. Soc

Conference Date: 22-26 Aug. 1994 Conference Location: Singapore

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Ray tracing is one of the computer graphics techniques used to render high quality images. Unfortunately, the ray tracing of complex scenes can require large amounts of CPU time, making the technique impractical for everyday use. Since the ray tracing calculations that **determine** the **values** of individual **pixels** are independent, this appears to be an easy problem to parallelize, and parallel algorithms have been proposed. However, **pixel** computation times can vary significantly, and naive attempts at parallelization give poor speedup due to the load imbalance between the **processors** . The key to achieving high **parallel** efficiency is to ensure that the computational load is evenly balanced. In this paper, we propose two new load balancing schemes and evaluate their performance for ray tracing on **parallel processors** . We term the new methods 'local distributed control' (LDC) and 'global distributed control' (GDC). Our new strategies are complementary: GDC performs forms well for high computational complexity images and LDC works well for low computational complexity images. (13 Refs)

Subfile: C

Descriptors: computational complexity; distributed control; parallel

algorithms; ray tracing; rendering (computer graphics); resource allocation
Identifiers: load balancing strategies; ray tracing; **parallel processors** ; computer graphics; high quality image rendering; complex scenes; CPU time; parallel algorithms; **pixel** computation times; parallelization; speedup; parallel efficiency; local distributed control; global distributed control; computational complexity
Class Codes: C6130B (Graphics techniques); C4240C (Computational complexity); C4240P (Parallel programming and algorithm theory); C6150N (Distributed systems software)

9/5/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

4548815 INSPEC Abstract Number: B9401-6140C-277, C9401-1250-198
Title: Image-data-based matching for affine transformed pictures
Author(s): Nomura, Y.; Harada, Y.; Fujii, S.
Author Affiliation: Dept. of Inf. Eng., Nagoya Univ., Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.1827 p.97-104
Publication Date: 1993 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
U.S. Copyright Clearance Center Code: 0 8194 1028 4/93/$4.00
Conference Title: Model-Based Vision
Conference Sponsor: SPIE
Conference Date: 19-20 Nov. 1992 Conference Location: Boston, MA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Theoretical (T); Experimental (X)
Abstract: The authors present a simple and robust pattern matching algorithm working on image-data level and requiring no feature extraction. A model picture is transformed into an estimated picture, and the estimated picture is matched to an actually input picture. Both the geometrical affine transformation and a linear grey-level transformation are examined, and the transformation parameters relating to the rotation, translation, expansion, and brightness are estimated by using a statistical optimization technique i.e., an iterative nonlinear least squares method where the residual sum of squares between the actually input picture and the estimated picture is used as an evaluation function. The characteristic of the proposed picture is that the parameters are estimated by linear matrices calculation so that the calculation is markedly simplified and it could be **processed** in **parallel** for all the **pixels** . As a result of some experiments for a simple pattern and a complicated one, it is **confirmed** that a translation parameter **value** is accurately estimated with approximately 0.1 **pixel** . The dynamics of parameter estimation is also examined. (5 Refs)
Subfile: B C
Descriptors: computer vision; image recognition; least squares approximations; optimisation; parameter estimation
Identifiers: image-data-based matching; computer vision; object recognition; affine transformed pictures; pattern matching algorithm; geometrical affine transformation; linear grey-level transformation; transformation parameters; rotation; translation; expansion; brightness; statistical optimization technique; iterative nonlinear least squares method; linear matrices calculation; parameter estimation
Class Codes: B6140C (Optical information and image processing); C1250 (Pattern recognition); C5260B (Computer vision and picture processing)

9/5/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

04378560 INSPEC Abstract Number: C9305-7840-004
Title: Understanding system of topographic map by multi-angled parallelism

Author(s): Yamada, H.; Yamamoto, K.; Saito, T.; Muraki, S.
Journal: Bulletin of the Electrotechnical Laboratory vol.56, no.9 p.104-35
Publication Date: 1992 Country of Publication: Japan
CODEN: DESIA7 ISSN: 0366-9092
Language: Japanese Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P)
Abstract: Feature extraction from topographic maps is important to utilize map information in a computer; however, it is difficult because there is much overlapping of information. There are two kinds of geometric features in topographic maps; one is indefinite formed linear feature such as road and railway which has arbitrary length, and the other is definite formed symbol which indicates a type of building and numerals. These two features are extracted and recognized by parallel calculation on directional feature field using MAP (multi-angled parallelism) concept. The MAP operation which is an erosion-dilation operation on directional feature field extracts the former indefinite formed linear feature. The MAP matching method extracts the definite formed symbols. In the MAP matching method input information is also expressed on the same directional field. The solution at every **pixel** is accumulated by parallel computation of translation and addition. The authors show the elevation value in the topographic map is recognized by a combination of the MAP operation and the MAP matching. Both results are integrated to **determine** the **value** , position and attribute of the elevation in the topographic map. (30 Refs)
Subfile: C
Descriptors: cartography; feature extraction; image recognition; **parallel processing**
Identifiers: feature extraction; multi-angled parallelism; topographic maps; geometric features; indefinite formed linear feature; definite formed symbol; parallel calculation; directional feature field; MAP; erosion-dilation operation; elevation value
Class Codes: C7840 (Geography and cartography); C5260B (Computer vision and picture processing)

9/5/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03763144 INSPEC Abstract Number: B90078106, C90069910
Title: Parallel distance transforms on pyramid machines: theory and implementation
Author(s): Borgefors, G.; Hartmann, T.; Tanimoto, S.L.
Author Affiliation: Swedish Defence Res. Establ., Linkoping, Sweden
Journal: Signal Processing vol.21, no.1 p.61-86
Publication Date: Sept. 1990 Country of Publication: Netherlands
CODEN: SPRODR ISSN: 0165-1684
U.S. Copyright Clearance Center Code: 0165-1684/90/$3.50
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: The authors present a parallel algorithm for weighted distance transforms that runs particularly efficiently on hierarchical cellular-logic machines, a subclass of the architectures known as pyramid machines. The algorithm computes the 3-4 distance transform. The algorithm runs in O(M) time, for an M*M image. Since it avoids using arithmetic except to maintain a counter, it is well-suited to the bit-serial **processor** architectures common in massively-**parallel** image **processing** . The algorithm updates the wave of distance **values** by repeatedly **checking** if any of each **pixel** 's neighbors have particular markings. A memory-efficient variant of the algorithm is also presented; here the upper levels of the pyramid are employed to restrict the ranges of values that finer-level cells can take on. The result is that only four bit-pyramids are necessary to represent arbitrarily large distance maps with the 3-4 distance, and only two bits are necessary for the chessboard distance. (32 Refs)
Subfile: B C
Descriptors: computerised picture processing; parallel algorithms;

transforms
Identifiers: binary images; pyramid machines; parallel algorithm; weighted distance transforms; hierarchical cellular-logic machines; bit-serial processor architectures; image processing; 3-4 distance; chessboard distance
Class Codes: B6140C (Optical information processing); C5260B (Computer vision and picture processing); C1250 (Pattern recognition)

9/5/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

03698594 INSPEC Abstract Number: C90057250
Title: PC board with i860: a superfast 64-bit parallel computer
Author(s): Klein, R.-D.; Thiel, T.
Journal: Mikrocomputer Zeitschrift no.6 p.94-105
Publication Date: June 1990 Country of Publication: West Germany
CODEN: MDMZDL ISSN: 0720-4442
Language: German Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The authors consider the software needed for operation and peripherals. They discuss and describe: the boot EPROM, the Assembler, the loading program, IO communications and the dual port RAM HD 63310. They give special emphasis to (3D) graphics by describing the commands needed by the **graphics unit** (Z-buffer **check** commands, **pixel** storage, **pixel** addition, Z-buffer interpolation and OR with merge register). They comment on using the software to generate a Mandelbrot diagram. The program listings are available on diskette. (0 Refs)
Subfile: C
Descriptors: **parallel processing**
Identifiers: 3D graphics; PC board; i860; superfast 64-bit parallel computer; software; boot EPROM; Assembler; loading program; IO communications; dual port RAM HD 63310; Z-buffer check commands; **pixel** storage; **pixel** addition; Z-buffer interpolation; Mandelbrot diagram; 64 bit
Class Codes: C5440 (Multiprocessor systems and techniques)
Numerical Indexing: word length 6.4E+01 bit

9/5/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

02742808 INSPEC Abstract Number: B86057991, C86047813
Title: A high speed two-dimensional digital filter structure
Author(s): Ty, K.M.; Venetsanopoulos, A.N.
Author Affiliation: Dept. of Electr. Eng., Toronto Univ., Ont., Canada
Conference Title: Conference Proceedings. 28th Midwest Symposium on Circuits and Systems p.441-4
Editor(s): Cole, J.D.; Miller, E.J.
Publisher: Univ. Louisville, Louisville, KY, USA
Publication Date: 1985 Country of Publication: USA 812 pp.
Conference Sponsor: Univ. Louisville
Conference Date: 19-20 Aug. 1985 Conference Location: Louisville, KY, USA
Availability: Western Periodicals, North Hollywood, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); New Developments (N); Theoretical (T); Experimental (X)
Abstract: A new digital filter structure is developed for the realization of two-dimensional (2-D) recursive filters for real-time image processing. The proposed architecture has a high data throughput rate independent of the order of the filter. Parallelism and pipelining are the two features of the new filter structure that contribute to its high speed performance. Hardware of the filter utilizing memories is briefly outlined. Using standard integrated circuits and memories, the new filter is capable of

processing images of size up to 512*512 **pixels** with a TV scan rate of 30 frames/sec in real-time. The effects of finite precision arithmetic are considered. Simulation results are obtained to **check** the **validity** of the error expressions derived. (4 Refs)
Subfile: B C
Descriptors: **parallel processing** ; picture processing; pipeline processing; two-dimensional digital filters
Identifiers: 2 D digital filters; **parallel processing** ; hardware; image size 512*512 **pixels** ; digital filter structure; recursive filters; real-time image processing; high data throughput rate; pipelining; high speed performance; filter utilizing memories; standard integrated circuits; TV scan rate of 30 frames/sec; finite precision arithmetic; error expressions
Class Codes: B1270F (Digital filters); B6140C (Optical information processing); C5240 (Digital filters); C5440 (Multiprocessor systems and techniques)

9/5/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

01752446 INSPEC Abstract Number: C81031384
Title: Language and architecture for parallel **image** processing
Author(s): Sternberg, S.R.
Author Affiliation: Environmental Res. Inst. of Michigan, Ann Arbor, MI, USA
Conference Title: Pattern Recognition in Practice. Proceedings of an International Workshop p.35-44
Editor(s): Gelsema, E.S.; Kanal, L.N.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1980 Country of Publication: Netherlands xii+552 pp.
ISBN: 0 444 86115 7
Conference Date: 21-23 May 1980 Conference Location: Amsterdam, Netherlands
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: Cytocomputer image processing operations are based on the concepts of cellular automata. Each cell or **picture element** of an image is subjected to a sequence of time discrete transformations, the transformed **value** of a cell being **determined** by the initial **values** of a finite group of cells composing its neighborhood. Each image transformation is performed in a individual cytocomputer processing element referred to as a processing stage. A cytocomputer consists of a serial pipeline of programmable processing stages, where each stage in the pipeline performs a single transformation on a entire image. Pictures are entered into a cytocomputer in a line-scanned format and progress through the pipeline of processing stages at the same rate they are scanned. (11 Refs)
Subfile: B C
Descriptors: computer architecture; computerised pattern recognition; **parallel processing**
Identifiers: **parallel** image **processing** ; cellular automata; neighborhood; cytocomputer; serial pipeline; line-scanned format; computerised pattern recognition; **parallel processing** ; digital processor; space event
Class Codes: B6140C (Optical information processing); C1250 (Pattern recognition); C5530 (Pattern recognition equipment)

9/5/10 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04131338 E.I. No: EIP95042651415
Title: Load balancing strategies for ray tracing on parallel

processors
Author: Lee, Tong-Yee; Raghavendra, C.S.; Nicholas, John B.
Corporate Source: Washington State Univ, Pullman, WA, USA
Conference Title: Proceedings of the 1994 IEEE Region 10's 9th Annual International Conference (TENCON'94). Part 1 (of 2)
Conference Location: Singapore, Singapore Conference Date: 19940822-19940826
Sponsor: IEEE Region 10; IEEE Singapore Section; Institution of Engineers, Singapore
E.I. Conference No.: 42774
Source: Frontiers of Computer Technology IEEE Region 10's Annual International Conference, Proceedings v 1 1995. IEEE, Piscataway, NJ, USA,94CH3417-3. p 177-181
Publication Year: 1995
CODEN: 001989
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical)
Journal Announcement: 9506W1
Abstract: Ray tracing is one of the computer graphics techniques used to render high quality images. Unfortunately, ray tracing complex scenes can require large amounts of CPU time, making the technique impractical for everyday use. Since the ray tracing calculations that **determine** the **values** of individual **pixels** are independent, this appears to be an easy problem to parallelize and parallel algorithms have been proposed. However, **pixel** computation times can vary significantly, and naive attempts at parallelization give poor speedup due to load imbalance between the **processors** . The key to achieving high **parallel** efficiency is to ensure that the computational load is evenly balanced. In this paper, we propose two new load balancing schemes and evaluate the performance of ours for ray tracing on **parallel processors** . We term both new methods Local Distributed Control (LDC) and Global Distributed Control (GDC). Our new strategies are complementary: GDC performs well for high computational complexity images and LDC works well for low computational complexity images. (Author abstract) 13 Refs.
Descriptors: Computer graphics; **Parallel processing** systems; **Parallel** algorithms; Image quality; Computational complexity; Calculations ; Efficiency; Performance; Image processing
Identifiers: Load balancing; Ray tracing; **Pixels** ; Local distributed control method; Global distributed control method
Classification Codes:
723.5 (Computer Applications); 722.4 (Digital Computers & Systems); 723.1 (Computer Programming); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 723.2 (Data Processing)
723 (Computer Software); 722 (Computer Hardware); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING)

9/5/11 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03597656 E.I. Monthly No: EI9305064718
Title: Simulation and verification of associative processor arrays.
Author: Duller, A. W. G.; Storer, R.
Corporate Source: Univ of Wales, Bangor, Irel
Source: Parallel Computing v 18 n 12 Dec 1992 p 1403-1414
Publication Year: 1992
CODEN: PACOEJ ISSN: 0167-8191
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical); A; (Applications)
Journal Announcement: 9305
Abstract: This work is based on the design of a VLSI processor array comprising single bit processing elements combined with Content Addressable

Memory (CAM) left bracket 1,2 right bracket . The processors are connected in a linear array with 64 currently being combined on a chip. Each processor is linked to 64 bits of data CAM and 4 bits of subset CAM (used for marking subsets of the array for subsequent processing). The architecture is targeted at image applications including **pixel** based processing as well as higher level symbolic manipulation and incorporates a data shift register linking all of the processing elements which allows data loading and processing to occur concurrently. The current situation is that an extensive functional simulation package has been written left bracket 3 right bracket which allows algorithms to be coded and executed on a system which comprises an arbitrary number of array chips together with its controlling hardware. This allows algorithms to be investigated, and tuned to the architecture. A reduced design has been fabricated and the chips are undergoing parametric testing. A full version of the processor array chip will then be produced allowing a complete image system to be tested. The VLSI design work undertaken so far left bracket 2 right bracket shows that the blocks with the design can easily be replicated an arbitrary number of times (subject to chip size constraints) to create an application specific CAM array. The need for this type of flexibility has been borne out by the algorithmic work that has been carried out by a number of workers. In order to make the design of application specific arrays possible it is vital that the simulation tools are fast enough to allow adequate testing to be performed on the new design. It is for this reason that the original simulation package, written in C, has been transferred onto a transputer array. This paper looks at the way in which the simulation is mapped onto the transputers in such a way that an arbitrary number can be used. In addition the problems of **verification** and **validation** of the simulator and the VLSI design are addressed. Results are given for a number of different applications which show very encouraging speed-ups. In many ways it has been found that the efficiency with which the simulation can be carried out with a large number of transputers mirrors the efficiency of the processor array in terms of communications overhead. (Author abstract) 9 Refs.

Descriptors: **PARALLEL PROCESSING** SYSTEMS; COMPUTER SIMULATION; ASSOCIATIVE STORAGE; IMAGE PROCESSING

Identifiers: CONTENT-ADDRESSSABLE MEMORY

Classification Codes:

722 (Computer Hardware); 723 (Computer Software); 741 (Optics & Optical Devices)

72 (COMPUTERS & DATA PROCESSING); 74 (OPTICAL TECHNOLOGY)

9/5/12 (Item 1 from file: 94)

02571007 JICST ACCESSION NUMBER: 95A0492235 FILE SEGMENT: JICST-E

Acceleration of iterative image reconstruction using a massively parallel processor.

IKEMOTO HIROYUKI (1); OGAWA KOICHI (1)
(1) Hosei Univ., Coll. of Eng.

Keisan Denki, Denshi Kogaku Shinpojiumu Ronbunshu, 1995, VOL.15th, PAGE.209-212, FIG.5, TBL.1, REF.5
JOURNAL NUMBER: L0026AAB
UNIVERSAL DECIMAL CLASSIFICATION: 681.3:621.397.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

ABSTRACT: The image reconstruction method using ML-EM(Maximum Likelihood method using Expectation Maximization) algorithm is a kind of stochastic approach, and is useful when acquired projection data is incomplete. However the method is not practical because of computation time. In this paper, we proposed two parallel computation algorithms using a massively parallel computer CM-5E. In this study we developed two message-passing programs; one is a **pixel** oriented program and the other is a bin oriented one. These two methods were **evaluated** and the

validity of **parallel processing** in image reconstruction was also discussed. (author abst.)
DESCRIPTORS: emission CT; maximum likelihood method; image reproduction; distributed processing; sequential processing; fast algorithm; computer architecture; computer simulation; expectation value; maximum problem; speedup; **parallel processing** ; parallel computer; image reconstruction; massively parallel computers
BROADER DESCRIPTORS: computed tomography; diagnostic imaging; diagnosis; tomography; image technology; technology; scintigraphy; radioisotope diagnosis; radiographic inspection; nondestructive inspection; inspection; statistical estimation; estimation; statistical decision; decision; statistical method; image processing; information processing; treatment; regeneration; computer algorithm; algorithm; computer system(architecture); method; computer application; utilization; simulation; statistic; mean value; numerical value; optimization problem; problem; modification; improvement; digital computer; computer ; hardware
CLASSIFICATION CODE(S): JE04010I

9/5/13 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02326056 JICST ACCESSION NUMBER: 95A0483498 FILE SEGMENT: JICST-E
Parallel Calculation Algorithm in-ML-EM Image Reconstruction.
IKEMOTO HIROYUKI (1); OGAWA KOICHI (1)
(1) Hosei Univ., Coll. of Eng.
Hosei Daigaku Keisan Senta Kenkyu Hokoku(Bulletin of Computer Center, Hosei University), 1995, VOL.8, PAGE.49-54, FIG.4, TBL.2, REF.4
JOURNAL NUMBER: L0821AAW ISSN NO: 0913-8420
UNIVERSAL DECIMAL CLASSIFICATION: 681.3:621.397.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The image reconstruction method using ML-EM(Maximum Likelihood method using Expectation Maximization) algorithm is a kind of stochastic approach, and is useful when acquired projection data is incomplete. However the method is not practical because of computation time. In this paper, we proposed two parallel computation algorithms using a massively parallel computer CM-5E. In this study we developed two message-passing programs; one is a **pixel** oriented program and the other is a bin oriented one. These two methods were **evaluated** and the **validity** of **parallel processing** in image reconstruction was also discussed. (author abst.)
DESCRIPTORS: image reproduction; maximum likelihood method; **parallel processing** ; parallel arithmetic; algorithm; image reconstruction
BROADER DESCRIPTORS: image processing; information processing; treatment; regeneration; statistical estimation; estimation; statistical decision; decision; statistical method; arithmetic system; method
CLASSIFICATION CODE(S): JE04010I

9/5/14 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02257016 JICST ACCESSION NUMBER: 95A0101416 FILE SEGMENT: JICST-E
On-sensor Motion Estimation.
ONO HIROSHI (1); HAMAMOTO TAKAYUKI (1); AIZAWA KIYOHARU (1); HATORI MITSUTOSHI (1)
(1) Univ. of Tokyo, Fac. of Eng.
Terebijon Gakkai Gijutsu Hokoku, 1994, VOL.18,NO.68(IPU94 63-73/IDY94 166-176), PAGE.7-12, FIG.7, REF.6
JOURNAL NUMBER: S0209AAF ISSN NO: 0386-4227
UNIVERSAL DECIMAL CLASSIFICATION: 681.3:621.397.3

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In this paper, an architecture of imagers which execute motion estimation on the focal plane is proposed. Since the motion estimation needs quite heavy **processing** , the proposed **parallel** architecture can effectively reduce the total processing time and circuit complexity. A kind of single **pixel** matching is employed in this algorithm. **Validity** of this algorithm is **confirmed** by simulations. We also propose one of its component circuits: MOS resistor with segmentation switch. (author abst.)
DESCRIPTORS: image compression; image sensor; parallel arithmetic; **pixel** ; resistance circuit; computational complexity; segmentation(computer); switching circuit; analog method; moving image; MOS structure; register ; pattern matching; image correction; coding(signal); motion compensation; image coding
BROADER DESCRIPTORS: image processing; information processing; treatment; image pickup apparatus; equipment; arithmetic system; method; image; circuit; device structure; matching(graph); matching; correction(compensation); correction(modification); modification; signal processing; compensation
CLASSIFICATION CODE(S): JE04010I

9/5/15 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01328728 JICST ACCESSION NUMBER: 91A0687669 FILE SEGMENT: JICST-E
Discrimination of Rotated Textural Images Jointly Using Two PDP Models.
UMEDA MICHIO (1)
(1) Osaka Electro-Communication Univ., Faculty of Engineering
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1991, VOL.91,NO.156(PRU91 42-50), PAGE.17-24, FIG.4, REF.2
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 681.3:165
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A new discrimination system of textural images is proposed. In this system, two statistical features named a gray level co-occurrence matrix and a gray level difference feature are independently used. These features are extracted from an arbitrary 64*64 **pixels** area or four 32*32 **pixels** areas and consist of 80 elements. An artificial neural network based on a **parallel** distributed **processing** model is utilized for each feature and a category of maximum output **value** is **determined** as a descrimination result. The experimental result shows that this system can perfectly discriminate 10 types of natural textural images which contain unrotated and 90-degree rotated ones. (author abst.)
DESCRIPTORS: image understanding; texture processing; pattern recognition; feature extraction; computer vision; learning; **parallel processing** ; video camera; resolving power; aerial photography; **pixel** ; similarity
BROADER DESCRIPTORS: image processing; information processing; treatment; recognition; extraction; separation; computer application; utilization; camera; optical instrument; image pickup apparatus; equipment; performance; photography; image; property
CLASSIFICATION CODE(S): JE07000S

9/5/16 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00731054 JICST ACCESSION NUMBER: 89A0417868 FILE SEGMENT: JICST-E

A threshold selection method based on the mean of adjacent number in binary images.

SASAKAWA KOUICHI (1); KURODA SHIN-ICHI (1); IKEBATA SHIGEKI (1)
(1) Mishibishidenki Sangyoshisutemuken

Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1989, VOL.89,NO.73(PRU89 19-26), PAGE.49-56(PRU89-25), FIG.10, REF.9
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 681.3:621.397.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

ABSTRACT: Thresholding is a general method for image segmentation, and many approaches have been using the gray level histogram as a guide of threshold selection. A different approach is to **determine** the optimal threshold by **checking validity** of each binary image when the thrshold varies. We propose a similar method that selects the appropriate threshold at which "compact" regions are extracted from the binary image. We define the mean of adjacent number as a measure of "compactness", and find the threshold for which this measure is a local maximum. This method works well even under difficult conditions such as a noisy image containing small objects.(author abst.)

DESCRIPTORS: image processing; **parallel processing** ; halftone image; **pixel** ; computer algorithm; computer simulation; threshold
BROADER DESCRIPTORS: information processing; treatment; image; algorithm; computer application; utilization; simulation; numerical value
CLASSIFICATION CODE(S): JE04000X

13/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01558190 E.I. Monthly No: EI8409091657 E.I. Yearly No: EI84061604
Title: REAL-TIME LAPLACIAN IMAGE EDGE DETECTOR ON A SINGLE VLSI CHIP.
Author: Anastassiou, D.; Georgiou, C. J.
Source: IBM Technical Disclosure Bulletin v 26 n 11 Apr 1984 p 5947-5953
Publication Year: 1984
CODEN: IBMTAA ISSN: 0018-8689
Language: ENGLISH
Journal Announcement: 8409
Abstract: A single chip Laplacian image edge detector is described which can perform the Laplacian operation A0 MINUS 1/8*(A1 PLUS A2 PLUS . . . PLUS A8) on every picture element (pixel) of a 512 X 512 digital image in real time. The chip consists of an array M X N of **processing** elements (PEs) which operate in **parallel** . A picture is divided into regions of M X N pixels which are loaded into the chip from the picture buffer via **multiple** serial paths. The **pixels** are distributed throughout the chip so that each PE receives one pixel. The PEs consist roughly of a single-bit adder, two **shift registers** , two multiplexers, nine tri-state buffers to control near-neighbor communication, a latch and other control logic.
Descriptors: *IMAGE PROCESSING--*Equipment; INTEGRATED CIRCUITS, VLSI
Identifiers: IMAGE EDGE DETECTORS
Classification Codes:
741 (Optics & Optical Devices); 723 (Computer Software); 713 (Electronic Circuits); 714 (Electronic Components)
74 (OPTICAL TECHNOLOGY); 72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

13/5/2 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1004389 NTIS Accession Number: AD-A122 104/3
Architectures and Algorithms for Parallel Updates of Raster Scan Displays
(Doctoral thesis)
Gupta, S.
Carnegie-Mellon Univ., Pittsburgh, PA. Dept. of Computer Science.
Corp. Source Codes: 005343001; 403081
Report No.: CMU-CS-82-111
Dec 81 174p
Languages: English Document Type: Thesis
Journal Announcement: GRAI8308
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A08/MF A01
Country of Publication: United States
Contract No.: F33615-78-C-1551; ARPA ORDER-3597
The frame buffer memory organization is the key to achieving high display performance. Traditional frame buffer designs use the scan-line organization which allows **several pixels** along the length of a scan-line to be updated together. This thesis advocates the symmetric square organization which allows the access of square regions of the display. This organization is based on the belief that the regions of the display which are commonly accessed simultaneously are no more likely to be tall and thin than to be short and wide. The square memory organization is studied for representative display applications and is shown to be indeed better than the scan-line organization. Based on the algorithms for these applications, a display design is presented. This design uses one custom designed LSI chip, 64 copies of which are required to implement the frame buffer memory system. (Author)
Descriptors: Computer graphics; *Display systems; *Memory devices; Line

scanning; Rasters; Modification; Algorithms; Chips(Electronics); Two dimensional; **Shift registers** ; Buffer storage; **Parallel processing** ; Image **processing** ; Formats; Computer architecture; Arrays; Theses
Identifiers: LSI(Large Scale Integration); Pixels; NTISDODXA
Section Headings: 62B (Computers, Control, and Information Theory--Computer Software); 62A (Computers, Control, and Information Theory--Computer Hardware)

13/5/3 (Item 1 from file: 108)
DIALOG(R)File 108:AEROSPACE DATABASE

02387822 N98-21085
NICMOS data processing software in STSDAS
Busko, Ivo C. (Space Telescope Science Inst., Baltimore, MD United States)
NASA no. 19980202061. The 1997 HST Calibration Workshop with a New Generation of Instruments.
Jan. 1997
REPORT NO.: NASA no. 19980202061
LANGUAGE: English
COUNTRY OF ORIGIN: United States COUNTRY OF PUBLICATION: United States
DOCUMENT TYPE: CONFERENCE PAPER
DOCUMENTS AVAILABLE FROM AIAA Technical Library
JOURNAL ANNOUNCEMENT: STAR9801
Until now the standard form of accessing observational data from the Hubble Space Telescope was through Generic Environmental Impact Statement (GEIS) or Servicing Test Facility (STF) files. The GEIS format was designed to allow storage of multiple "images" in a single file. The files, however, must store the same kind of information, e.g. science pixels, data quality **flags** , etc. If a given instrument generates, e.g., both science and data quality arrays, they must be stored in separate files. The new HST instruments Space Telescope Imaging Spectrograph (STIS) and Near Infrared Camera and **Multi** -Object Spectrometer (NICMOS) generate **several** "**pixel** " arrays from each exposure. Besides the usual science and data quality arrays, there is an error array, and NICMOS includes additional exposure time and number of samples arrays. It would be impractical to store all this associated information in separate files. In order to keep all information pertaining to a single exposure packed together in a single file, the standard data format adopted for STIS and NICMOS data files is FITS with multiple extensions. Each associated "chunk" of information is named an IMSET, and a single file can store multiple IMSETs, each one identified by a number stored in the EXTVER keyword in each FITS extension header. The existing Interactive Data Reduction and Analysis Facility (IRAF) and STSDAS tasks can operate upon individual FITS extensions as individual images with no problems, but in this way it becomes extremely cumbersome to properly propagate the error, data quality and other information from the input IMSETs into the result. Thus the need for brand-new tasks that could perform basic image **processing** and at the **same time** automatically propagate the associated information. This paper describes the mstools package, the NICMOS package, Basic image processing, and image statistics
DESCRIPTORS: *CAMERAS; *NEAR INFRARED RADIATION; *DATA PROCESSING; *HUBBLE SPACE TELESCOPE; *IMAGE PROCESSING; *IMAGING TECHNIQUES; *APPLICATIONS PROGRAMS (COMPUTERS); DATA REDUCTION; EXPOSURE; PIXELS; IMAGING SPECTROMETERS
SUBJECT CLASSIFICATION: 7561 Computer Programming & Software (1975-)

19/5/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04633306 JICST ACCESSION NUMBER: 00A0019597 FILE SEGMENT: JICST-E
A Robot Control Library of a Robot System for RoboCup SmallSize League. JP/S-II Project.
KOSUE SHOGO (1); IGARASHI HARUKAZU (1); TANAKA KAZUMOTO (1); MIYOSHI TAKANORI (1); **KUROSE YOSHINOBU** (1)
(1) Kinki Univ.
Nippon Robotto Gakkai Gakujutsu Koenkai Yokoshu, 1999, VOL.17th,dai2bunsatsu, PAGE.551-552, FIG.1, TBL.2, REF.2
JOURNAL NUMBER: X0008AAR
UNIVERSAL DECIMAL CLASSIFICATION: 007.52:681.51
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes a robot control library in our JP/S-II project being developed at Kinki University. The JP/S-II system consists of robots (on-board system) and its control system (off-board system). The off-board system consists of 3 components: **Image Processing** Server that recognizes robots' positions and postures by **processing images** from a video camera above the field, Remote Brains that control robots and Communication Server that controls communication among robots and Remote Brains. We prepared a robot control library for users of the JP/S-II system. The library functions will make it easier to develop programs in Remote Brains. (author abst.)
DESCRIPTORS: mobile robot; software development; library(computer); motion control; remote control; soccer; multiagent system
IDENTIFIERS: RoboCup
BROADER DESCRIPTORS: robot; computer system development; development; software; control; sports; computer application system; system
CLASSIFICATION CODE(S): IC04012J

19/5/2 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04525408 JICST ACCESSION NUMBER: 00A0227791 FILE SEGMENT: JICST-E
The present state and problem of JP/S-II robot system.
KOSUE SHOGO (1); IGARASHI HARUKAZU (1); MIYOSHI TAKANORI (1); IIDOI SHUICHI (1); **KUROSE YOSHINOBU** (1)
(1) Kinki Univ., Fac. of Eng.
Jinko Chino Gakkai AI Charenji Kenkyukai Shiyo(JSAI Technical Report), 1999, VOL.6th, PAGE.58-63, FIG.10, TBL.5, REF.6
JOURNAL NUMBER: L1884CAM
UNIVERSAL DECIMAL CLASSIFICATION: 007.52:681.51 681.3:165
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
DESCRIPTORS: mobile robot; computer vision; **image processing** system; client server system; remote control; library(computer); performance evaluation; positioning; accuracy
IDENTIFIERS: RoboCup
BROADER DESCRIPTORS: robot; computer application; utilization; computer application system; system; computer system(hardware); control; software; evaluation; degree
CLASSIFICATION CODE(S): IC04012J; JE07000S

19/5/3 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04190568 JICST ACCESSION NUMBER: 99A0639287 FILE SEGMENT: JICST-E
Image Processing **Server in a Robot System for RoboCup Small Size League. JP/S-II Project.**
TANAKA KAZUMOTO (1); KOSUE SHOGO (1); IGARASHI HARUKAZU (1); **KUROSE YOSHINOBU** (1); ASAOKA TADASHI (2)
(1) Kinki Univ., Fac. of Eng.; (2) Kyotokodogijutsuken
Jinko Chino Gakkai AI Charenji Kenkyukai Shiyo(JSAI Technical Report), 1999, VOL.4th, PAGE.1-4, FIG.6, REF.5
JOURNAL NUMBER: L1884CAM
UNIVERSAL DECIMAL CLASSIFICATION: 681.3:621.397.3 007.52:681.51 681.3:165
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
DESCRIPTORS: pattern recognition; robot; computer vision; center of gravity; positioning; intelligent robot; error(measure)
BROADER DESCRIPTORS: recognition; computer application; utilization; position
CLASSIFICATION CODE(S): JE04010I; IC04012J; JE07000S

19/5/4 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03950691 JICST ACCESSION NUMBER: 99A0270550 FILE SEGMENT: JICST-E
Construction of Learning Support System with WWW.
KUROSE YOSHINOBU (1)
(1) Kinki Univ., Fac. of Eng.
Kinki Daigaku Kogakubu Kenkyu Hokoku(Research Reports of the Faculty of Engineering, Kinki University), 1998, NO.32, PAGE.127-136, FIG.15, TBL.1, REF.9
JOURNAL NUMBER: G0851AAM ISSN NO: 0386-491X
UNIVERSAL DECIMAL CLASSIFICATION: 681.3.02:37 681.3:654
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Studies about teaching support and learning support using a computer network are carried out flourishingly. Author proposed the 3D-CAD learning support system and the collaboration design training support system, and implemented these system and utilized in a lecture of university. Through these research, author explained the problems at building the learning support system using internet. This paper settles past research result and describes a policy to construct nice learning environment. (author abst.)
DESCRIPTORS: internet; WWW(communication); learning; CAI; CAL; cooperative work; client server system; duplex communication; **image processing**
BROADER DESCRIPTORS: computer network; communication network; information network; network; information system; computer application system; system; education and training; computer application; utilization; groupware; application program; computer program; software; computer system(hardware); communication system; method; information processing; treatment
CLASSIFICATION CODE(S): JE09000G; JC03000K

19/5/5 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01808041 JICST ACCESSION NUMBER: 93A0616994 FILE SEGMENT: JICST-E
Evaluation of Air Temperature Distribution using Thermal Image under Conditions of Nocturnal Radiative Cooling in Winter Season over Shikoku

Area.
KUROSE YOSHITAKA (1); HAYASHI YOSEI (1)
(1) Shikoku National Agricultural Exp. Stn.
Nogyo Kisho(Journal of Agricultural Meteorology), 1993, VOL.49,NO.1, PAGE.11-17, FIG.7, REF.10
JOURNAL NUMBER: X0731AAK ISSN NO: 0021-8588
UNIVERSAL DECIMAL CLASSIFICATION: 551.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: Using the thermal images offered by the infra-red thermometer and the LANDSAT, the air temperature distribution over mountainous regions were estimated under conditions of nocturnal radiative cooling in the winter season. The thermal image analyses by using an infra-red thermometer and the micrometeological observation were carried out around Zentsuji Kagawa prefecture. At the same time, the thermal image analyses were carried out by using the LANDSAT data. The LANDSAT data were taken on Dec. 7, 1984 and Dec. 5, 1989. The scenes covered the west part of Shikoku, southwest of Japan. The results were summarized as follows: Values of the surface temperature of trees, which were measured by an infra-red thermometer, were almost equal to the air temperature. On the other hand, DN values detected by LANDSAT over forest area were closely related with air temperature observed by AMeDAS. Therefore, it is possible to evaluate instantaneously a spatial distribution of the nocturnal air temperature from thermal image. The LANDSAT detect a surface temperature over Shikoku area only at 21:30. When radiative cooling was dominant, the thermal belt and the cold air lake were already fromed on the mountain slopes at 21:30. Therefore, it is possible to estimate the characteristic of nocturnal temperature distribution by using LANDSAT data. It became clear that the temperature distribution estimated by thermal images offered by the infra-red thermometer and the LANDSAT was useful for the evaluation of rational land use for winter crops. (author abst.)
DESCRIPTORS: Shikoku District; winter; radiative cooling; **image processing** ; night; thermography; geodetic satellite; remote sensing; air temperature distribution; sloping land; mountainous region; agricultural meteorology
BROADER DESCRIPTORS: Japan; East Asia; Asia; season; cooling; information processing; treatment; image technology; technology; thermal test; inspection; applications satellite; artificial satellite; space craft; flying object; distribution; land; meteorological phenomenon
CLASSIFICATION CODE(S): DC05010D

19/5/6 (Item 6 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00036840 JICST ACCESSION NUMBER: 85A0102801 FILE SEGMENT: JICST-E
The three dimentional motion analysis of the hand of cerebral palsy.
MUNESHIGE HIROSHI (1); KATAYAMA AKITARO (1); **KUROSE YASURO** (1); TAKEMOTO MASATADA (1); KANDA TSUKASA (1); TAKADA SHOGO (1); TSUSHITA TAKEYA (2)
(1) Hiroshimakenshintaishogaisharihabirise; (2) Hiroshima Univ., School of Medicine
Chubu Nippon Seikei Geka Saigai Geka Gakkai Zasshi(Central Japan Journal of Orthopaedic & Traumatic Surgery), 1984, VOL.27,NO.4, PAGE.1441-1444, FIG.2, TBL.1, REF.4
JOURNAL NUMBER: Z0420BAS ISSN NO: 0008-9443
UNIVERSAL DECIMAL CLASSIFICATION: 616.7-07
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
DESCRIPTORS: VTR; image analysis; medical equipment; cerebral palsy; hand(body region); movement physiology; clinical trial; computer application system; pathophysiology

. BROADER DESCRIPTORS: magnetic tape recorder; magnetic recorder; recording equipment; equipment; video recorder; **image processing** ; information processing; treatment; analysis(separation); analysis; brain disease; central nervous system disease; nervous system disease; disease; paralytic disease; arm(forefoot); extremity; body region; motion; test; system

CLASSIFICATION CODE(S): GG02000M

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File  16:Gale Group PROMT(R) 1990-2001/Jun 07
         (c) 2001 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2001/Jun 07
         (c)2001 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2001/Jun 07
         (c) 2001 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2001/Jun 07
         (c) 2001 The Gale Group
File  88:Gale Group Business A.R.T.S. 1976-2001/Jun 08
         (c) 2001 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2001/Jun 07
         (c) 2001 The Gale group
File 275:Gale Group Computer DB(TM) 1983-2001/Jun 07
         (c) 2001 The Gale Group

Set     Items   Description
S1     102035   PIXEL? OR PEL OR PELS OR SUBPIXEL? OR PICTURE()ELEMENT?
S2       2206   (PLURAL? OR MANY OR MULTI OR MULTIPLE OR MANY OR NUMEROUS -
            OR SEVERAL OR MORE(1W)ONE)(5W)S1
S3      95077   (SIMULTAN? OR SAME()TIME OR AT()ONCE OR TOGETHER OR PARALL-
            EL)(5N)(PROCESS??? OR PERFORM?(2N)OPERATION?)
S4    3448459   VALID? OR VALUE? ? OR S1(5N)(POLYGON? OR SHAPE? ? OR TRIAN-
            GLE? OR PRIMITIVE? OR GRAPHIC???(2W)UNIT? ?)
S5     123264   (CHECK? OR VERIF? OR MONITOR? OR CONFIRM? OR AUTHENTIC? OR
            JUDG? OR DETERMIN? OR EVALUAT?)(5N)S4
S6          0   S2(S)S3(S)S5
S7          0   S1(S)S3(S)S5
S8     166553   FLAG? ? OR FLAGG? OR SHIFT(2W)REGISTER?
S9       1046   (CLOCK? ?(5N)SIGNAL????) AND (STOP? ? OR STOPP? OR HALT? OR
             TERMINAT? OR ABORT? OR DEACTIVAT? OR DE()ACTIVAT? OR CONTROL-
            ?)(5N)(PROCESS??? OR OPERATION?)
S10         0   S2(S)S3(S)S8
S11         0   S2(S)S3(S)S9
S12         7   S1(S)S3(S)(S8 OR S9)
S13         4   RD (unique items)
?
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13/3,K/1 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

06155285 Supplier Number: 53956276 (USE FORMAT 7 FOR FULLTEXT)
CPU And Memory Advances Propel Chips To New Performance Heights.
Bursky, Dave
Electronic Design, v47, n4, p46(1)
Feb 22, 1999
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 3884

... tap long FIR filter; performance of a 256-point or larger DFT or FFT; or many other standard DSP operations.
Targeted at real-time, pixel-**parallel** image **processing** , a 1-Mbit content-addressable memory (CAM) was developed jointly by the NTT Integrated Information and Energy Systems Laboratories, Atsugi, Japan, and the NTT Human...

...word by 64-bit block of associative memory cells. The chip includes functions for search or parallel writes with upward/downward mask shift and hit-**flag** counting. When clocked at 40 MHz, the chip can perform a 64-bit search in just 25 ns, or an 8-bit, four-neighbor interword...

13/3,K/2 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

05857699 SUPPLIER NUMBER: 12184249 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Silicon solution merges video, stills, and voice; codec chip set drives standard algorithms for desktop multimedia and videoconferencing. (AT and T AVP1000 video-codec chip set) (includes a related article on compression algorithms) (Cover Story)
Leonard, Milt
Electronic Design, v40, n7, p45(6)
April 2, 1992
DOCUMENT TYPE: Cover Story ISSN: 0013-4872 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2473 LINE COUNT: 00204

... bit-rate mode allows the user to set the quantizastion-step size. The quantization processor is also responsible for buffer management.
The encoder's signal **processor** consists of a **controller** circuit and six **processors** organized in a single-instruction, multiple-data (SIMD) architecture. The six **processors** operate in **parallel** on the 8-by-8-**pixel** blocks, performing such functions as discrete cosine transformations (DCTs), quantization, zig-zag scanning, inverse discrete cosine transformations (IDCTs), as well as inverse quantization.
Information produced...

13/3,K/3 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03134193 SUPPLIER NUMBER: 04959894 (USE FORMAT 7 OR 9 FOR FULL TEXT)
CMOS four-chip set processes images at 20-MHz data rates.
Bursky, Dave
Electronic Design, v35, p39(5)
May 28, 1987
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2728 LINE COUNT: 00202

... 64, 8-by-128, etc.) can also be selected.
ADJUST THE TRANSFER RATE

Providing the elasticity between the various blocks, the variable-length delay line (**shift register**) allows designers to trade off data size with the number of lines or the register length in any power of 2. Moreover, it can turn a 1D video signal into a 2D matrix for **parallel processing** . The L64210 is organized as four 8-bit-wide **shift registers** , each 1024 **pixels** deep (each **pixel** is represented by an 8-bit value). The L64211, has double the number of outputs but half the length for each register--eight 8-bit wide channels, each 512 **pixels** deep (Fig. 4).

Each delay line acts as a variable-length shift register by using a block of RAM. Read and write pointers are generated...

13/3,K/4 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01516851 SUPPLIER NUMBER: 12213457 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Multimedia - here today, not tomorrow. (AT&T Microelectronics' AVP1000 video chip set)(Technology Directions: Computers & Subsystems)
Wilson, Dave
Computer Design, v31, n4, p56(3)
April, 1992
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1374 LINE COUNT: 00111

... system controller.

Both versions of the encoder are composed of 10 functional blocks. First, there's a host bus interface that synchronizes the host bus **signals** to the main input **clock** . Then, there's an uncompressed data FIFO used to hold the chrominance and luminance **pixel** data until it's written into the frame store DRAM. An on-chip memory controller arbitrates access to the frame store DRAM and provides a...

...processor to determine the quantization step size and output frame rate. The signal processor itself comprises no fewer than six SIMD (Single Instruction Multiple Data) **processors** that work in **parallel** - performing functions such as discrete cosine transformations (DCTs), quantization and zigzag scan. The global **controller** sequences the **operation** of the other blocks to ensure that data dependency requirements between them are satisfied. A variable-length encoder operates on the information produced by the...

```
?show files;ds
File  15:ABI/Inform(R) 1971-2001/Jun 08
         (c) 2001 ProQuest Info&Learning
File  98:General Sci Abs/Full-Text 1984-2001/Apr
         (c) 2001 The HW Wilson Co.
File 674:Computer News Fulltext 1989-2001/May W4
         (c) 2001 IDG Communications
File 624:McGraw-Hill Publications 1985-2001/Jun 07
         (c) 2001 McGraw-Hill Co. Inc
File   9:Business & Industry(R) Jul/1994-2001/Jun 07
         (c) 2001 Resp. DB Svcs.
File  75:TGG Management Contents(R) 86-2001/May W4
         (c) 2001 The Gale Group
File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 612:Japan Economic Newswire(TM) 1984-2001/Jun 08
         (c) 2001 Kyodo News
File 635:Business Dateline(R) 1985-2001/Jun 08
         (c) 2001 ProQuest Info&Learning
File 484:Periodical Abs Plustext 1986-2001/May W4
         (c) 2001 ProQuest
File 647:CMP  Computer Fulltext 1988-2001/Jun W1
         (c) 2001 CMP
File 623:Business Week 1985-2001/Jun W2
         (c) 2001 The McGraw-Hill Companies Inc
File  20:World Reporter 1997-2001/Jun 08
         (c) 2001 The Dialog Corporation

Set     Items   Description
S1      35675   PIXEL? OR PEL OR PELS OR SUBPIXEL? OR PICTURE()ELEMENT?
S2        686   (PLURAL? OR MANY OR MULTI OR MULTIPLE OR MANY OR NUMEROUS -
            OR SEVERAL OR MORE(1W)ONE)(5W)S1
S3      53759   (SIMULTAN? OR SAME()TIME OR AT()ONCE OR TOGETHER OR PARALL-
            EL)(5N)(PROCESS??? OR PERFORM?(2N)OPERATION?)
S4    3125448   VALID? OR VALUE? ? OR S1(5N)(POLYGON? OR SHAPE? ? OR TRIAN-
            GLE? OR PRIMITIVE? OR GRAPHIC???(2W)UNIT? ?)
S5     101185   (CHECK? OR VERIF? OR MONITOR? OR CONFIRM? OR AUTHENTIC? OR
            JUDG? OR DETERMIN? OR EVALUAT?)(5N)S4
S6          0   S2(S)S3(S)S5
S7          0   S1(S)S3(S)S5
S8     195649   FLAG? ? OR FLAGG? OR SHIFT(2W)REGISTER?
S9        191   (CLOCK? ?(5N)SIGNAL????) AND (STOP? ? OR STOPP? OR HALT? OR
             TERMINAT? OR ABORT? OR DEACTIVAT? OR DE()ACTIVAT? OR CONTROL-
            ?)(5N)(PROCESS??? OR OPERATION?)
S10         0   S2(S)S3(S)S8
S11         0   S2(S)S3(S)S9
S12         2   S1(S)S3(S)(S8 OR S9)
S13         2   RD (unique items)
```

13/3,K/1 (Item 1 from file: 370)
DIALOG(R)File 370:Science

00500807 (USE 9 FOR FULLTEXT)
Accessing Genetic Information with High-Density DNA Arrays
Chee, Mark; Yang, Robert; Hubbell, Earl; Berno, Anthony; Huang, Xiaohua C.; Stern, David; Winkler, Jim; Lockhart, David J.; Morris, Macdonald S.; Fodor, Stephen P. A.
Affymetrix, 3380 Central Expressway, Santa Clara, CA 95051, USA.
Science Vol. 274 5287 pp. 610
Publication Date: 10-25-1996 (961025) Publication Year: 1996
Document Type: Journal ISSN: 0036-8075
Language: English
Section Heading: Reports
Word Count: 3285

(THIS IS THE FULLTEXT)

...Text: developed a two-color labeling and detection scheme in which the reference is labeled with phycoerythrin (red), and the target with fluorescein (green) (B13) . By **processing** the reference and target **together** , experimental variability during the fragmentation, hybridization, washing, and detection steps is minimized or eliminated. In addition, during cohybridization of the reference and target, competition for...

...To read polymorphisms accurately, we developed an algorithm that addresses the issue of multiple mismatches. The algorithm performs base identification but also **flags** regions of ambiguity caused by multiple mismatches. These regions are easily identified by the presence of a large footprint (Fig. 2, B and C) or...

...more bases identified as differing from P.sup(0) within the span of a single probe. Discrepancies between base identifications and footprint patterns are also **flagged** for further analysis (for example, a P.sup(0) footprint in which no polymorphism is identified; such a pattern is typical of a deletion). Thus, base identifications are valid only for unflagged regions. In **flagged** regions, the presence of sequence differences is detected, but no attempt is made to identify the sequence without further analysis...

...correctly (B17) . The remaining 2% of the sequence, which contained the multiple substitution footprints (such as those shown in Fig. 2, B and C), was **flagged** for further analysis. Of the 649 bp composing this 2%, 643 bp were located in or immediately adjacent to footprints (B18) . In all, 179 out of the 180 polymorphisms were unambiguously detected, 126 out of 127 were identified correctly in the unflagged regions, and 53 polymorphisms occuring in the **flagged** regions were detected as footprints. There were no unflagged false-positive base identifications, and only one false-positive footprint. These figures can be considered to...Although there is considerable sequence-dependent intensity variation, most of the array can be read directly. The image was collected at a resolution of ~100 **pixels** per probe cell. (C) The ability of the array to detect and read single-base differences in a 16.6-kb sample is illustrated. Two...

13/3,K/2 (Item 1 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

04949261 SUPPLIER NUMBER: 66987996 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Global lightning variations caused by changes in thunderstorm flash rate and by changes in the number of thunderstorms
Williams, E; Rothkin, K; Stevenson, D; Boccippio, D
Journal of Applied Meteorology (IJAM), v39 n12, p2223-2230, p.8
Dec 2000

ISSN: 0894-8763 JOURNAL CODE: IJAM
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 5401

TEXT:

... and any flash within 22 km (along latitude and longitude lines) of the initial flash is then assigned to an existing "area." Data processing limitations (**flagged** in the OTD data file) may cause this clustering rule to be violated up to 20%--30% of the time in the OTD data (based on these **flags**). LIS areas are defined similarly; any flash not within 16.5 km of a previous or **simultaneous** flash initiates an area.' **Processing** limitations do not affect application of the LIS clustering algorithm. Because the typical OTD/LIS view time is much shorter than a thunderstorm lifetime, no lifetime is assigned to an "area." The 22-km scale (16.5 for LIS), which admittedly is comparable to the **pixel** size of the measurement (8-13 km for om, 3-6 km for LIS) was chosen to bound the size of the majority of isolated...

File 348:EUROPEAN PATENTS 1978-2001/May W02
(c) 2001 European Patent Office
File 349:PCT Fulltext 1983-2001/UB=20010531, UT=20010517
(c) 2001 WIPO/MicroPat

Set	Items	Description
S1	43717	PIXEL? OR PEL OR PELS OR SUBPIXEL? OR PICTURE()ELEMENT?
S2	9234	(PLURAL? OR MANY OR MULTI OR MULTIPLE OR MANY OR NUMEROUS - OR SEVERAL OR MORE(1W)ONE)(5W)S1
S3	45981	(SIMULTAN? OR SAME()TIME OR AT()ONCE OR TOGETHER OR PARALL-EL)(5N)(PROCESS??? OR PERFORM?(2N)OPERATION?)
S4	438455	VALID? OR VALUE? ? OR S1(5N)(POLYGON? OR SHAPE? ? OR TRIAN-GLE? OR PRIMITIVE? OR GRAPHIC???(2W)UNIT? ?)
S5	98529	(CHECK? OR VERIF? OR MONITOR? OR CONFIRM? OR AUTHENTIC? OR JUDG? OR DETERMIN? OR EVALUAT?)(5N)S4
S6	19	S2(S)S3(S)S5
S7	13	S6 NOT (STARTCODE OR START()CODE)/TI
S8	42515	FLAG? ? OR FLAGG? OR SHIFT(2W)REGISTER?
S9	18779	(CLOCK? ?(5N)SIGNAL????) AND (STOP? ? OR STOPP? OR HALT? OR TERMINAT? OR ABORT? OR DEACTIVAT? OR DE()ACTIVAT? OR CONTROL-?)(5N)(PROCESS??? OR OPERATION?)
S10	14	S2(S)S3(S)S8
S11	8	S10 NOT S6
S12	10	S9(S)S2(S)S3
S13	5	S12 NOT (S6 OR S10)
S14	10	AU=(KUROSE YOSH?)
S15	9	S14 NOT (S6 OR S10 OR S12)
S16	0	S15 AND S1
S17	6	AU=KUROSE YOSHIKAZU?
S18	5	S17 NOT (S6 OR S10 OR S12)

7/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01077085
Image processing apparatus and method
Bildverarbeitungsvorrichtung und -verfahren
Appareil et methode de traitement d'image
PATENT ASSIGNEE:
SONY CORPORATION, (214022), 7-35, Kitashinagawa 6-chome Shinagawa-ku, Tokyo, (JP), (Applicant designated States: all)
INVENTOR:
Kurose, Yoshikazu, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Thevenet, Jean-Bruno et al (39781), Cabinet Beau de Lomenie 158, rue de l'Universite, 75340 Paris Cedex 07, (FR)
PATENT (CC, No, Kind, Date): EP 947978 A2 991006 (Basic)
EP 947978 A3 991229
APPLICATION (CC, No, Date): EP 99400838 990406;
PRIORITY (CC, No, Date): JP 9891844 980403; JP 9951795 990226
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G09G-005/00
ABSTRACT WORD COUNT: 118
NOTE:
Figure number on first page: 3

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9940	2732
SPEC A	(English)	9940	11597
Total word count - document A			14329
Total word count - document B			0
Total word count - documents A + B			14329

...ABSTRACT power consumption by a large extent, wherein a predetermined shape to be displayed on a display is expressed by a composite of unit graphics by **performing operations** on a **plurality** of **pixels** **simultaneously** and by performing **processing** on valid results of operations for pixels positioned inside a unit graphic being processed. Clock enablers (2101)) to 2151)), ... 2108)) to 2158))) in operation sub-blocks (2001)) to 2051)), ... 2008)) to 2058))) **judge** the **validity** of the corresponding val data (S2201)), ..., S2208))). Only operation sub-blocks receiving the corresponding val data indicating validity perform operations. Other operation sub-blocks do...

...SPECIFICATION expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a **plurality** of **pixels** positioned within the same graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within the graphic unit to be processed among pixel data of a **plurality** of **pixels** to be **processed** **simultaneously** , the image **processing** apparatus comprising a pixel position judging circuit for **judging** whether or not a corresponding **pixel** is positioned within the **graphic** **unit** for each of the **plurality** of **pixel** data to be **processed** **simultaneously** ; a **plurality** of **pixel** **processing** circuits for processing a **plurality** of **pixel** data to be **processed** **simultaneously** mutually in **parallel** ; and a control circuit for stopping the operation of the pixel processing circuits other than processing circuits for processing pixel data of pixels positioned within the graphic unit to be processed among the **plurality** of **pixel** processing circuits on the basis of the results of the judgement of the pixel position judging circuit.
According to a third aspect of the present...

...expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a **plurality** of **pixels** positioned within the same graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within the graphic unit to be processed among pixel data of a **plurality** of **pixels** to be **processed simultaneously**, the image **processing** apparatus comprising a plurality of image processing circuits, provided for a **plurality** of **pixels** to be **processed simultaneously**, for blending a **plurality** of first **pixel** data and a corresponding **plurality** of second **pixel** data by a blending ratio indicated by blending ratio data set for each pixel to produce a **plurality** of third **pixel** data and a control circuit for **judging** whether or not a corresponding **pixel** is positioned within a **graphic unit** for each of the **plurality** of **pixels** to be **processed simultaneously** and stopping the operation of a pixel processing circuit when **judging** that the corresponding **pixel** is not positioned within the **graphic unit** or when **judging** that the blending will not be performed on the basis of the blending ratio data.

According to a fifth aspect of the present invention, there...

...expressing an image to be display on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a **plurality** of **pixels** positioned within the same graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within the graphic unit to be processed among pixel data of a **plurality** of **pixels** to be **processed simultaneously**, the image **processing** apparatus comprising a storage circuit; a **plurality** of **pixel** processing circuits, provided for a **plurality** of **pixels** to be **processed simultaneously**, for producing a **plurality** of second **pixel** data from a **plurality** of first **pixel** data; a comparing circuit for comparing a plurality of the first depth data of the **plurality** of first **pixel** data and a plurality of second depth data of a **plurality** of third **pixel** data stored in the storage circuit in correspondence with the plurality of first depth data; and a control circuit for **judging** whether or not a corresponding **pixel** is positioned within the **graphic unit** for each of the **plurality** of **pixels** to be **processed simultaneously**, judging whether or not to rewrite the third pixel data corresponding to the second depth data stored in the storage circuit with the second pixel data on the basis of the result of the comparison, and stopping the operation of a pixel processing circuit when **judging** that the corresponding **pixel** is not positioned within the **graphic unit** or when **judging** not to rewrite.

According to a seventh aspect of the present invention, there is provided an image processing method for performing image processing by using...

...expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a **plurality** of **pixels** positioned within the same graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within the graphic unit to be processed among pixel data of a **plurality** of **pixels** to be **processed simultaneously**, the image **processing** method comprising **judging** whether or not a corresponding **pixel** is positioned within the **graphic unit** for each of the **plurality** of **pixel** data to be **processed simultaneously**; **processing** a **plurality** of **pixel** data to be **processed simultaneously** mutually in **parallel** in a **plurality** of **pixel processing** circuits: and stopping the operation of the pixel processing circuits other than processing circuits for processing pixel data of pixels positioned within the graphic unit to be processed among the **plurality** of **pixel** processing circuits on the basis of the results of the judgement.

According to a ninth aspect of the present invention, there is provided an image...

...expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a **plurality** of **pixels** positioned within the same graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within the graphic unit to be processed among pixel data of a **plurality** of **pixels** to be **processed simultaneously** , the image **processing** method comprising using a plurality of image processing circuits, provided for a **plurality** of **pixels** to be **processed simultaneously** , to blend a **plurality** of first **pixel** data and a **plurality** of second **pixel** data by a blending ratio indicated by blending ratio data set for each pixel to produce a **plurality** of third **pixel** data and **judging** whether or not a corresponding **pixel** is positioned within a **graphic unit** for each of the **plurality** of **pixels** to be **processed simultaneously** and stopping the operation of a pixel processing circuit when **judging** that the corresponding **pixel** is not positioned within the **graphic unit** or when **judging** that the blending will not be performed on the basis of the blending ratio data.

According to an 11th aspect of the present invention, there...

...expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a **plurality** of **pixels** positioned within the same graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within the graphic unit to be processed among pixel data of a **plurality** of **pixels** to be **processed simultaneously** , the image **processing** method comprising using a **plurality** of **pixel** processing circuits, provided for a **plurality** of **pixels** to be **processed simultaneously** , to produce a **plurality** of second **pixel** data from a **plurality** of first **pixel** data; comparing a plurality of the first depth data of the **plurality** of first **pixel** data and a plurality of second depth data of a **plurality** of third **pixel** data stored in a storage circuit in correspondence with the plurality of first depth data; and **judging** whether or not a corresponding **pixel** is positioned within the **graphic unit** for each of the **plurality** of **pixels** to be **processed simultaneously** , judging whether or not to rewrite the third pixel data corresponding to the second depth data stored in the storage circuit with the second pixel data on the basis of the result of the comparison, and stopping the operation of a pixel processing circuit when **judging** that the corresponding **pixel** is not positioned within the **graphic unit** or when **judging** not to rewrite.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become clearer from the following description...

...CLAIMS be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a pixel position judging circuit for **judging** whether or not a corresponding **pixel** is positioned within said **graphic unit** for each of the plurality of pixel data to be **processed simultaneously** ;

a **plurality** of **pixel processing** circuits for processing a plurality of pixel data to be processed simultaneously mutually in parallel; and

a control circuit for stopping the operation of the...

...a blending ratio indicated by blending ratio data set for each pixel to produce a plurality of third pixel data and

a control circuit for **judging** whether or not a corresponding **pixel** is positioned within a **graphic unit** for each of said **plurality** of **pixels** to be **processed simultaneously** and stopping the operation of a pixel processing circuit when **judging** that said corresponding **pixel** is not positioned within said **graphic unit** or when **judging** that said blending will not be performed on the

basis of said blending ratio data.

11. An image processing apparatus comprising:
a storage circuit;
a...a plurality of third pixel data stored in said storage circuit in correspondence with said plurality of first depth data; and
a control circuit for **judging** whether or not a corresponding **pixel** is positioned within said **graphic unit** for each of said **plurality** of **pixels** to be **processed simultaneously** , judging whether or not to rewrite said third pixel data corresponding to said second depth data stored in said storage circuit with said second pixel data on the basis of the result of the comparison, and stopping the operation of a pixel processing circuit when **judging** that said corresponding **pixel** is not positioned within said **graphic unit** or when **judging** not to rewrite.

16. An image processing method for performing image processing by using pixel processing circuits, each provided for each of a plurality of ...

...graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:
judging whether or not a corresponding **pixel** is positioned within said **graphic unit** for each of the **plurality** of **pixel** data to be **processed simultaneously** ;
processing a plurality of pixel data to be processed simultaneously mutually in parallel in a plurality of pixel processing circuits; and

stopping the operation of the...of second pixel data by a blending ratio indicated by blending ratio data set for each pixel to produce a plurality of third pixel data,
judging whether or not a corresponding **pixel** is positioned within a **graphic unit** for each of said **plurality** of **pixels** to be **processed simultaneously** and
stopping the operation of a pixel processing circuit when judging that said corresponding pixel is not positioned within said graphic unit or when judging...

...second depth data of a plurality of third pixel data stored in a storage circuit in correspondence with said plurality of first depth data; and
judging whether or not a corresponding **pixel** is positioned within said **graphic unit** for each of said **plurality** of **pixels** to be **processed simultaneously** , judging whether or not to rewrite said third pixel data corresponding to said second depth data stored in said storage circuit with said second pixel...

7/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01042789
Printing head system and graphic data transferring method
Druckkopfsystem und Verfahren zur Ubertragung von graphischen Daten
Systeme de tete d'impression et methode de transfert de donnees graphiques
PATENT ASSIGNEE:
TOYO INK MANUFACTURING CO., LTD., (403750), No. 3-13, Kyobashi 2-chome Chuo-ku, Tokyo, (JP), (applicant designated states: AT;BE;CH;CY;DE;DK;ES;FI;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
INVENTOR:
Castegnier, Adrien, 36 Beloeil, Outremont, Quebec H2V 2Z2, (CA)
Castegnier, Guy, 6C, Ferland 120, Iles des Soeurs (Verdun), Quebec H3E 1L1, (CA)
Castegnier, Pierre, 10890 Tolhurst, Montreal, Quebec H3L 3A7, (CA)
Goyette, Charles, 758 Bienville, Montreal, Quebec H2J 1T3, (CA)
LEGAL REPRESENTATIVE:
Koepe, Gerd L. (59775), Koepe, Fiesser & Partner GBR, Radeckestrasse 43

EG, D-81245 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 922586 A1 990616 (Basic)
APPLICATION (CC, No, Date): EP 98123404 981209;
PRIORITY (CC, No, Date): CA 2224339 971210
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: B41J-002/39; B41C-001/10;
ABSTRACT WORD COUNT: 144

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9924	907
SPEC A	(English)	9924	5701
Total word count - document A			6608
Total word count - document B			0
Total word count - documents A + B			6608

...SPECIFICATION pixel density correction device for processing a signal containing pixel density values conveyed to a printing head of an electrocoagulation printing apparatus that includes a **plurality** of simultaneously addressable electrodes, said **pixel** density correction device including: an input for receiving said signal representative of pixel density values associated with said **simultaneously** addressable electrodes; and a signal **processing** element for altering a pixel density value of a selected one of said **simultaneously** addressable electrodes, said signal **processing** element being responsive to pixel density values associated with electrodes other than said selected electrode to **determine** a corrected pixel density **value** associated with said selected electrode.
According to further aspect of the present invention, there is provided a method of correcting pixel density, comprising the steps...

...CLAIMS pixel density correction device for processing a signal containing pixel density values conveyed to a printing head of an electrocoagulation printing apparatus that includes a **plurality** of simultaneously addressable electrodes, said **pixel** density correction device including:
- an input for receiving said signal representative of pixel density values associated with said **simultaneously** addressable electrodes; and
- a signal **processing** element for altering a pixel density value of a selected one of said **simultaneously** addressable electrodes, said signal **processing** element being responsive to pixel density values associated with electrodes other than said selected electrode to **determine** a corrected pixel density **value** associated with said selected electrode.

11. A method of correcting pixel density, comprising the steps of:
(a) processing a signal containing pixel density values conveyed...

7/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00983604
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane Stichcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE,

(GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, GLoucester GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 891088 A1 990113 (Basic)
EP 891088 B1 010509
APPLICATION (CC, No, Date): EP 98202133 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 269
NOTE:
Figure number on first page: 38

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199902	662
CLAIMS B	(English)	200119	778
CLAIMS B	(German)	200119	770
CLAIMS B	(French)	200119	881
SPEC A	(English)	199902	126651
SPEC B	(English)	200119	120956
Total word count - document A			127332
Total word count - document B			123385
Total word count - documents A + B			250717

...SPECIFICATION critical path problems in the logic circuit. The elastic nature of the pipeline eliminates any centralized control since all the interworkings between the submodules are **determined** by a completely localized decision and, in addition, each submodule can autonomously perform data buffering and self-timed data-transfer control at the same time...a block diagram that illustrates a basic embodiment of a pipeline stage that incorporates a two-wire transfer control and also shows two consecutive pipeline **processing** stages with the two-wire transfer control;
Figures. 5a and 5b taken together depict one example of a timing diagram that shows the relationship between...structure of the color-space converter.

SUMMARY OF THE INVENTION
Briefly, and in general terms, the present invention provides an input, an output and a **plurality** of processing stages between the input and the output, the plurality of processing stages being interconnected by a two-wire interface for conveyance of tokens...

7/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00975324
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley,

Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucesterhire GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 884910 A1 981216 (Basic)
EP 884910 B1 010509
APPLICATION (CC, No, Date): EP 98202132 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 104
NOTE:
Figure number on first page: 76

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199851	498
CLAIMS B	(English)	200119	330
CLAIMS B	(German)	200119	308
CLAIMS B	(French)	200119	382
SPEC A	(English)	199851	126705
SPEC B	(English)	200119	122739
Total word count - document A			127222
Total word count - document B			123759
Total word count - documents A + B			250981

...SPECIFICATION of different type standard-dependent signals passing into the serial pipeline processor for handling. The technique used is to study all the parameters of the **multi** -standards that are selected for processing by the serial processor and noting 1) their similarities, 2) their dissimilarities, 3) their needs and requirements and 4...MPI should wait "after writing a 1 to a request access register" until 1 is read from the access register. If a user writes a **value** to a configuration register while its access register is set to zero, the results are undefined.

14. MICRO-PROCESSOR INTERFACE
A standard byte wide micro...multi-standard tokens. The first portion of the IDCT checks the entering data to ensure that the DATA tokens are of the correct size for **processing** . In fact, the token stream can be corrected in some situations if the error is not too large.

27. BUFFER MANAGER
The Buffer Manager of...

...ready for display. Once a buffer is displayed, the buffer is in a "vacant" state. When the Buffer Manager receives a PICTURE(underscore)START, FLUSH, **valid** or access token, it **determines** the status of each buffer and its readiness to accept new data. For example, the PICTURE(underscore)START token causes the Buffer Manager to cycle...

7/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00734704
Full text storage and retrieval in image at OCR and code speed

Volltext-Speicher- und -Suchverfahren in Bildern, mit einer OCR- und Code-Geschwindigkeit
Stockage et recherche plein texte dans les images, a une vitesse comparable a la vitesse des recherches OCR et code
PATENT ASSIGNEE:
FROESSL, Horst, (317950), Gutenbergstrasse 2-4, D-69502 Hemsbach, (DE), (applicant designated states: BE;CH;DE;ES;FR;GB;IT;LI;NL;SE)
INVENTOR:
Froessl, Horst, Gutenbergstrasse 2-4, D-6944 Hemsbach, (DE)
Farley, Walter C., 10513 Bucknell Drive, Wheaton, MD 20902, (US)
LEGAL REPRESENTATIVE:
Frei, Alexandra Sarah (49784), Frei Patentanwaltsburo Hedwigsteig 6 Postfach 768, CH-8029 Zurich, (CH)
PATENT (CC, No, Kind, Date): EP 692768 A2 960117 (Basic)
EP 692768 A3 970502
APPLICATION (CC, No, Date): EP 95110987 950713;
PRIORITY (CC, No, Date): US 276116 940715
DESIGNATED STATES: BE; CH; DE; ES; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: G06K-009/68;
ABSTRACT WORD COUNT: 296

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	1110
SPEC A	(English)	EPAB96	7651
Total word count - document A			8761
Total word count - document B			0
Total word count - documents A + B			8761

...SPECIFICATION arrangement of electronic bits stored in a memory as the result of storing the scanner output.
The method of the present invention involves constructing a **multiple** -layer, character- or word-structure, **pixel** -related code which will be referred to herein as a multiple "value code" to distinguish it from a conventional object code such as ASCII in...

...font. A test program can be used to determine per font the overlay of pixel splatter as shown in Fig. 2B. Each layer of the **value** code is **determined** by the on and off conditions of the pixels with a dark pixel typically being considered an "on" condition and a light pixel as "off". Layers are **determined** by **value** or search runs accomplished in **parallel** with each other to increase **processing** speed, the number and levels of the runs being used as required for individual recognition problems.
Referring to Figs. 1 and 2A, "run levels" are...

7/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00597615
Method of assigning a colour indication to picture elements in a colour reproduction system.
Verfahren zur Zuweisung einer Farbindikation zu Bildelementen in einem Farbeproduktionssystem.
Procede d'attribution d'une indication de couleur a des elements d'image dans un systeme de reproduction en couleurs.
PATENT ASSIGNEE:
Oce-Nederland B.V., (241030), St. Urbanusweg 43, NL-5914 CC Venlo, (NL), (applicant designated states: DE;FR;GB;NL)
INVENTOR:
Westdijk, Jacob Albert, Anne Frankstraat 193, NL-5912 HB Venlo, (NL)
Schonenberg, Jacobus Hendrikus Maria, Ooievaarstraat 6, NL-5941 JH Velden, (NL)
Sommer, Monique Gerardine Miranda, Schans 25, NL-5641 PP Eindhoven, (NL)

Onvlee, Johannes, Lamstraatje 4, NL-5211 DX 's-Hertogenbosch, (NL)
LEGAL REPRESENTATIVE:
Hanneman, Henri W.A.M. et al (49472), Oce-Nederland B.V. Patents and Information Postbus 101, NL-5900 MA Venlo, (NL)
PATENT (CC, No, Kind, Date): EP 593114 A1 940420 (Basic)
APPLICATION (CC, No, Date): EP 93202799 931001;
PRIORITY (CC, No, Date): NL 921761 921012
DESIGNATED STATES: DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: H04N-001/46;
ABSTRACT WORD COUNT: 166

LANGUAGE (Publication,Procedural,Application): English; English; Dutch
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	1891
SPEC A	(English)	EPABF2	7855
Total word count - document A			9746
Total word count - document B			0
Total word count - documents A + B			9746

...SPECIFICATION associated directional coefficient a*, and from that the COLfd value by reference to the measured L and C co-ordinates for each picture element, quicker **determination** of the COLfd **value** is obtained by means of a memory unit such as a look up table, which directly yields the associated COLfd value for each pair of...

...accordingly advantageous if picture elements having the picture errors due to this type of colour tinge are selected for their systematic character prior to or **simultaneously** with a picture element information **processing** method as described above, and to decide on whether or not there is a colourless behaviour in respect of these picture elements with suitable criteria...values (or intensity values) of the picture elements occurring therein are determined. Advantageously, the picture elements situated on an edge are not included in the **determination** of the brightness **value** in such a sub-raster. Of all the standard edges, that edge is selected where the difference between the maximum brightness value of one sub...

...edge. If a standard edge is considered as a potential black-white edge, the second step is started. In the second step, the average chroma **value** (Cmean1; Cmean2) is **determined** for that potential edge in each of the two sub-rasters, and from this an assessment is made as to whether there is a colour tinge present. Here again it is advantageous not to include in the **determination** of the average chroma **value** those picture elements which are situated on said potential edge. If the average chroma value of each of two sub-rasters remains below a certain...

...or colour-bearing where an opposite designation would be correct. This is because compromises must always be made in respect of the ideal processing when **determining** the critical **values** applied. In particular, in the case of black-white transitions, picture elements with a specific colour may be left over as a result of register...

...tested with a post-processing algorithm. According to this algorithm, a picture element considered to have colour behaviour can be rendered colourless if, for example, **many picture elements** having a pertinent indication of colourless behaviour occur in a certain environment of such picture element (and hence few picture elements having a pertinent indication...the line arrays. The successively arranged line arrays thus each deliver the intensity information of a single scanned point, and this is then used to **determine** the white reference **value** for each scanned point and each colour component for the line defined by the scanned points.
Instead of scanner it is also possible to use...

...suitable for processing colour information obtained via the correction phase in order to produce control signals for controlling a colour

printing unit 7 adapted to **multi** -colour printing. For each **picture element** , the colour components R, G, B measured by a scanner 5 are converted to the LCH colour system in unit 8. During this conversion, the ...

...9. The conversion then takes place to the LCH colour system as described in the said book by Hunt.

The white reference point should be **determined** accurately, since otherwise the grey **value** axis will be incorrectly **determined** in the LCH colour system so that the uncertainty area with the provisional indications of possible colourless or colour behaviour will be incorrectly disposed in...more practical approach of the process events is obtained if a number of process steps are performed independently of one another and to some extent **simultaneously** as shown in the picture **processing** and control unit illustrated in Fig. 5. Thus labelling according to the algorithm for the elimination of register errors in unit 10, determination of a...

...label, colourless label or provisional label for undefined colour behaviour in unit 14, and the "hue test" analysis in unit 15 can take place as **parallel processes** . A unit 16 receives and processes the results of the data to be supplied by units 14 and 15, in such manner that the data...

7/3,K/7 (Item 7 from file: 348)

00503101

WEB INSPECTION SYSTEM
GEWEBEBAND-INSPEKTIONSSYSTEM
SYSTEME D'INSPECTION DE BANDES

PATENT ASSIGNEE:
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PATENT (CC, No, Kind, Date): EP 520034 A1 921230 (Basic)
EP 520034 B1 960110
WO 9114173 910919
APPLICATION (CC, No, Date): EP 91907338 910313; WO 91US1666 910313
PRIORITY (CC, No, Date): US 493011 900313
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G01N-021/89; G06T-007/40;
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPAB96	868
CLAIMS B	(German)	EPAB96	872
CLAIMS B	(French)	EPAB96	1032
SPEC B	(English)	EPAB96	24125
Total word count - document A			0
Total word count - document B			26897
Total word count - documents A + B			26897

...SPECIFICATION the outputs of the twelve analog to digital converters into data streams for each strip of pixels which are fed to a shift memory holding **several** lines of **pixels** . Logic circuitry sums blocks of pixel values and compares with multiples of selected test pixel **values** to **determine** a defect. The above mentioned patents 3,781,117 and 4,752,897 detect transitions in the serial output signals and store

counts of pixel counters which are processed. The patent 4,752,897 utilizes four **parallel processors** to receive and **process** respective successive 64 byte segments of the stored data and transmit analysis data to a host computer.

The prior art also contains time delay integration...

7/3,K/8 (Item 8 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS
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00403519

Method and apparatus for removing noise data from a digitized image.
Verfahren und Einrichtung zur Rauschunterdruckung bei digitalisierten Bildern.
Methode et appareil pour l'elimination des bruits parasites d'une image digitalisee.

PATENT ASSIGNEE:
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LEGAL REPRESENTATIVE:
Kopacz, William James (52901), 83, Avenue Foch, F-75116 Paris, (FR)
PATENT (CC, No, Kind, Date): EP 401077 A2 901205 (Basic)
EP 401077 A3 921014
APPLICATION (CC, No, Date): EP 90401304 900516;
PRIORITY (CC, No, Date): US 354255 890518
DESIGNATED STATES: CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: G06F-015/68; H04N-001/40;
ABSTRACT WORD COUNT: 60

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	2189
SPEC A	(English)	EPABF1	9701
Total word count - document A			11890
Total word count - document B			0
Total word count - documents A + B			11890

...SPECIFICATION Figure 13 or some other image processing step. If the test of block 136 indicates that not all the pixels in the kernel have been **checked** for a **value** which exceeds the value of the pixel of interest, then a branch to block 130 is performed where each pair of aligned pixels in all the kernels are checked as previously described. Steps 130, 132, 134 and 136 are performed as **many** times as there are neighboring **pixels** to the pixel of interest in each kernel. These steps 130, 132 and 134 along with step 136 result in the **simultaneous processing** of the entire image.

Referring to Figure 15, there is shown a flowchart of the process represented by block 122 in Figure 13. This process...

7/3,K/9 (Item 1 from file: 349)

DIALOG(R)File 349:PCT Fulltext
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00802534

ANY-TO-ANY COMPONENT COMPUTING SYSTEM
SYSTEME INFORMATIQUE A COMPOSANTS TOUTE CATEGORIE

Patent Applicant/Assignee:
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Patent Applicant/Inventor:

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Legal Representative:
MEHRMAN Michael J (agent), Paper Mill Village, Building 23, 600 Village Trace, Suite 300, Marietta, GA 30067, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200135216 A2 20010517 (WO 0135216)
Application: WO 2000US31231 20001113 (PCT/WO US0031231)
Priority Application: US 99164884 19991112
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 291515

Fulltext Availability:
Detailed Description

Detailed Description
... invited me to come in.
Enabling a computer to determine when a user statement is complete.
Concept A useful method to enable a computer to **determine** if a statement is a Complete Statement or an Incomplete Statement [invite] is to state the behavior of Concept Symbols including Base

Concepts in terms...

7/3,K/10 (Item 2 from file: 349)
DIALOG(R)File 349:PCT Fulltext

00768013 **Image available**
VIDEO CAMERA WITH MAJOR FUNCTIONS IMPLEMENTED IN HOST SOFTWARE
CAMERA VIDEO A FONCTIONS PRINCIPALES MISES EN OEUVRE DANS UN LOGICIEL HOTE
Patent Applicant/Assignee:
LOGITECH INC, 6505 Kaiser Drive, Fremont, CA 94555-3615, US, US (Residence), US (Nationality)
Inventor(s):
HSU Mark, 101 Blaisdell Way, Fremont, CA 94536, US
NORCROSS Mitchell, 43511 Ocaso Corte, Fremont, CA 94539, US
AUBERGER Georges, 615 Palm Avenue, Los Altos, CA 94022, US
ZIMMERMANN Remy, 1549 Molitor Road, Belmont, CA 94022, US
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BILLERBECK Bryed, 441 Martens Avenue, Mountain View, CA 94040, US
LI Wei, 18820 Tilson Avenue, Cupertino, CA 95014, US
LABROUSSE Junien, 3750 Corina Way, Palo Alto, CA 94303, US
Legal Representative:
HAUGHEY Paul C, Townsend And Townsend And Crew LLP, Two Embarcadero Center, 8th Floor, San Francisco, CA 94111-3834, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 200101675 A2 20010104 (WO 0101675)
Application: WO 2000US18046 20000629 (PCT/WO US0018046)
Priority Application: US 99345167 19990630; US 99343934 19990630; US 99464364 19991215; US 2000602547 20000623
Designated States: CN (utility model) DE (utility model) KR
Publication Language: English
Filing Language: English

Fulltext Word Count: 12953

Fulltext Availability:
Detailed Description

Detailed Description
... register of the camera for later access by the host to perform corrections.

In one embodiment, the host decompresses the transmitted data by using a **processor** with the capability of **simultaneous** operations on **multiple** packed **pixel** values, such as the Intel MMXTM technology. This maintains a sufficient decompression speed for a larger amount of data with minimal impact on the frame...

...of bits from the data stream are duplicated and provided to multiple positions in a register, where they can be simultaneously compared to multiple maximuni. **values** . This allows a quick **determination** of how many bits of the variable bit encodini correspond to a pixel value.

In an embodiment using lossy compression, vignetting, garm-na, distortion or...

7/3,K/11 (Item 3 from file: 349)
DIALOG(R)File 349:PCT Fulltext

00717132 **Image available**
ADVANCED DEFERRED SHADING GRAPHICS PIPELINE PROCESSOR
PROCESSEUR PIPELINE GRAPHIQUE EVOLUE A OMBRAGE DIFFERE
Patent Applicant/Assignee:
APPLE COMPUTER INC, 1 Infinite Loop, Cupertino, CA 95014-2084, US, US (Residence), US (Nationality)
Inventor(s):
DULUK Jerome F Jr, 950 North California Drive, Palo Alto, CA 94303, US
HESSEL Richard E, 3225 Flemington Court, Pleasanton, CA 94588, US
ARNOLD Vaughn T, 621 Canepa Drive, Scotts Valley, CA 95066, US
BENKUAL Jack, 11661 Timber Spring Court, Cupertino, CA 95014, US
BRATT Joseph P, 1045 Oaktree Drive, San Jose, CA 95129, US
CUAN George, 798 Lusterleaf Drive, Sunnyvale, CA 94086, US
DODGEN Steven L, 15735 Forest Hill Drive, Boulder Creek, CA 95006, US
FANG Emerson S, 1197 Wisteria Drive, Fremont, CA 94539, US
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NG Sam, 34377 Maybird Circle, Fremont, CA 94555, US
PAPAKIPOS Matthew N, 1701 Oak Avenue, Menlo Park, CA 94025, US
REDGRAVE Jason R, 278 Martens Avenue, Mountain View, CA 95040, US
TRIVEDI Sushma S, 1208 Rembrandt Drive, Sunnyvale, CA 94087, US
TUCK Nathan D, 8666 Somerset Avenue, San Diego, CA 92123, US
GO Shun Wai, 370 Sandhurst Drive, Milpitas, CA 95035, US
FUNG Lindy, 358 Pescadero Terrace, Sunnyvale, Ca 94086, US
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MAMMEN Abraham, 2780 Lylewood Drive, Pleasanton, CA 94588, US
RASHID Abbas, 34369 Eucalyptus Terrace, Fremont, CA 94555-1982, US
TSAY Albert Suan-Wei, 38129 Cambridge Court, Fremont, CA 94536, US
Legal Representative:
ANANIAN R Michael, Flehr Hohbach Test Albritton & HerberT LLP, Suite 3400, 4 Embarcadero Center, San Francisco, CA 94111-4187, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 200030040 A1 20000525 (WO 0030040)
Application: WO 99US18971 19990820 (PCT/WO US9918971)
Priority Application: US 9897336 19980820; US 98213990 19981217

Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW SD SL SZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 181852

Fulltext Availability:
Detailed Description

Detailed Description
... these bits could designate the z-value or z-values to be accurate or conservative). While multiple z-values per sample can be easily used, **multiple** sets of primitive information per sample would be expensive.

Hereinafter, it is assumed that the SFSM maintains primitive information for one primitive. The SFSM may...CUL in the form of a Primitive Packet. CUL receives data from STP in tile order (in fact in the same order that STP receives **primitives** from SRT), and culls out or removes parts of the **primitives** that definitely do not contribute to the rendered images. (it may leave some parts of primitives if it cannot determine for certain that they will...

7/3,K/12 (Item 4 from file: 349)
DIALOG(R)File 349:PCT Fulltext
(c) 2001 WIPO/MicroPat. All rts. reserv.

00697194 **Image available**
TRILINEAR TEXTURE FILTERING WITH OPTIMIZED MEMORY ACCESS
FILTRAGE DE TEXTURES TRILINEAIRES AVEC ACCES MEMOIRE OPTIMISE
Patent Applicant/Assignee:
S3 INCORPORATED, S3 INCORPORATED, 2801 Mission College Boulevard, Santa Clara, CA 95052-8058, US
Inventor(s):
IOURCHA Konstantine I, IOURCHA, Konstantine, I., 310 Elan Village Lane &204, San Jose, CA 95134, US
LIAO Fred, LIAO, Fred, 4448 Canterbury Way, Union City, CA 94587, US
HONG Michael, HONG, Michael, 311 Checkers Drive &208, San Jose, CA 95133, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 0010126 A2 20000224 (WO 200010126)
Application: WO 99US18033 19990809 (PCT/WO US9918033)
Priority Application: US 9895994 19980810
Designated States: CA JP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Filing Language: English
Fulltext Word Count: 10962
Fulltext Availability:
Detailed Description

Detailed Description
... The steps of Fig. 15 are performed for each pixel being rendered in a given primitive, though in some embodiments, the steps are performed in **parallel** and **several pixels** may be **processed simultaneously** or consecutively. The preferred **process** begins in step 1501 by selecting a pixel indicated by a point P to be rendered on the display device 814. This will be done...

...e.g., 4x4) for the level id where id is the integer portion of the level of detail, d. Next in step 1504, the method **determines** a level I

channel **value** for the projection of point P on level id. This is preferably performed by bilinearly interpolating a value for the projection of point P on...

7/3,K/13 (Item 5 from file: 349)
DIALOG(R)File 349:PCT Fulltext

00283967
WEB INSPECTION SYSTEM
SYSTEME D'INSPECTION DE BANDES
Patent Applicant/Assignee:
EI DU PONT DE NEMOURS & COMPANY
Inventor(s):
GUAY Jean-Louis C
Patent and Priority Information (Country, Number, Date):
Patent: WO 9114173 A2 19910919
Application: WO 91US1666 19910313 (PCT/WO US9101666)
Priority Application: US 90493011 19900313
Designated States: AT BE CA CH DE DK ES FR GB GR IT JP LU NL SE
Publication Language: English
Fulltext Word Count: 29064

Fulltext Availability:
Detailed Description

Detailed Description
... the outputs of the twelve analog to digital converters into data streams for each strip of pixels which are fed to a shift memory holding **several** lines of **pixels** . Logic circuitry sums blocks of pixel values and compares with multiples of selected test pixel **values** to **determine** a defect. The above mentioned patents 3,781,117 and 4,752,897 detect transitions in the serial output signals and store counts of pixel counters which are processed. The patent 4,752,897 utilizes four **parallel processors** to receive and **process** respective successive 64 byte segments of the stored data and transmit analysis data to a host computer.

The prior art also contains time delay integration...
?

11/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00983606
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IE;IT;LI;NL)
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Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, CAM, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucestershire GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 891089 A1 990113 (Basic)
APPLICATION (CC, No, Date): EP 98202149 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 953013018)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-019/00; G06F-013/00; G06F-009/38;
ABSTRACT WORD COUNT: 165

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9902	165
SPEC A	(English)	9902	127403
Total word count - document A			127568
Total word count - document B			0
Total word count - documents A + B			127568

...SPECIFICATION down the pipeline.
The token may also be a CODING(underscore)STANDARD token for conditioning the system for processing in a selected one of a **plurality** of picture compression/decompression standards.
The CODING(underscore)STANDARD token may designate the picture standard as JPEG, andlor any other appropriate picture standard. At least...

11/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00484878
High-speed video camera.
Hochgeschwindigkeits-Videokamera.
Camera video a haute vitesse.
PATENT ASSIGNEE:
KABUSHIKI KAISHA N A C, (919221), No. 2-7, Nishiazabu 1-chome, Minato-Ku, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT;NL;SE)
INVENTOR:
Oguma, Kazuhiko, No. 2-1344-5,Sanno-Cho Kamimaruko,Nakahara-ku, Kawasaki-Shi,Kanagawa 211, (JP)

Suzuki, Hiroshi, No. 1-15, Asada 1-chome, Kawasaki-ku, Kawasaki-shi, Kanagawa, (JP)
Saito, Yutaka, No. 23-20, Senjumidori-cho 2-chome, Adachi-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Dealtry, Brian et al (42911), Eric Potter & Clarkson St. Mary's Court St. Mary's Gate, Nottingham NG1 1LE, (GB)
PATENT (CC, No, Kind, Date): EP 473259 A2 920304 (Basic)
EP 473259 A3 920527
EP 473259 B1 950927
APPLICATION (CC, No, Date): EP 91305583 910620;
PRIORITY (CC, No, Date): JP 90172077 900629; JP 9148706 910222
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: H04N-003/15;
ABSTRACT WORD COUNT: 179

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	655
CLAIMS B	(English)	EPAB95	609
CLAIMS B	(German)	EPAB95	537
CLAIMS B	(French)	EPAB95	722
SPEC A	(English)	EPABF1	2461
SPEC B	(English)	EPAB95	2182
Total word count - document A			3116
Total word count - document B			4050
Total word count - documents A + B			7166

...SPECIFICATION other side, the above-mentioned latter system has a shortcoming that it necessitates the specific solid-state image pickup element having mechanisms for delivering a **plurality** of **pixel** selecting pulses simultaneously from the same vertical **shift** **register** and for **processing** the obtained outputs **simultaneously** .
The present invention is aimed to furnish a high-speed video camera of a low cost which realizes high-speed scanning being the three time...

...SPECIFICATION other side, the above-mentioned latter system has a shortcoming that it necessitates the specific solid-state image pickup element having mechanisms for delivering a **plurality** of **pixel** selecting pulses simultaneously from the same vertical **shift** **register** and for **processing** the obtained outputs **simultaneously** .
In EP-A-0251790 there is described a solid-state imaging system with a vertical and/or horizontal window function in which the vertical and...

11/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00332029
APPARATUS AND METHODS FOR LOCATING EDGES AND DOCUMENT BOUNDARIES IN VIDEO SCAN LINES.
APPARAT UND VERFAHREN ZUM LOKALISIEREN VON RANDERN UND VORLAGENGRENZLINIEN IN VIDEOABTASTZEILEN.
APPAREIL ET PROCEDES POUR LOCALISER LES BORDS ET LES LIMITES D'UN DOCUMENT DANS DES LIGNES DE BALAYAGE VIDEO.
PATENT ASSIGNEE:
EASTMAN KODAK COMPANY (a New Jersey corporation), (201210), 343 State Street, Rochester New York 14650, (US), (applicant designated states: DE;GB)
INVENTOR:
MORTON, Roger, Roy, Adams, 157 Sawmill Road, Penfield, NY 14526, (US)
REDDEN, John, Edward, 32-E Hobbs Lane, Rochester, NY 14624, (US)
LEGAL REPRESENTATIVE:
Schmidt, Peter et al (50042), Kodak Aktiengesellschaft Postfach 600345 Hedelfinger Strasse, W-7000 Stuttgart 60, (DE)
PATENT (CC, No, Kind, Date): EP 331687 A1 890913 (Basic)

EP 331687 B1 921119
WO 8901268 890209
APPLICATION (CC, No, Date): EP 88906579 880705; WO 88US2252 880705
PRIORITY (CC, No, Date): US 77527 870724
DESIGNATED STATES: DE; GB
INTERNATIONAL PATENT CLASS: H04N-001/38; H04N-001/40;
ABSTRACT WORD COUNT: 271
NOTE:
No A-document published by EPO

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1931
CLAIMS B	(German)	EPBBF1	1258
CLAIMS B	(French)	EPBBF1	1656
SPEC B	(English)	EPBBF1	27342
Total word count - document A			0
Total word count - document B			32187
Total word count - documents A + B			32187

...SPECIFICATION table 4555.
A block diagram of noise detector and filter circuit 463, which forms part of image processing circuit 40 shown in FIGs. 2A and **2B** , is depicted in FIG. 9. As previously discussed, noise detector and filter circuit 463 determines whether any one of **several** **pre** -defined ... noise. Should a match occur between the pattern in the window and any pre-stored pattern, then a signal in the form of a "Noise **flag** " is provided over lead 465 to noise tracker 467. In addition, circuit 463 filters single pixel noise from the center pixel (changes its value) in ...

...table contains read only memories (ROMs) that store pre-defined noise patterns that could occur within a 3-by-3 window. Four different noise patterns **that** could occur within a 3-by-3 window are stored within the ROMs, but only one of these patterns is selected (by well known addressing...

...through flip-flops 4637 and 4639 in order to produce a pulse, which lasts two clock cycles, on lead 465. This pulse is the "Noise **flag** ". This pulse causes noise tracker 467 (see FIGs. 2A and 2B), which is discussed in detail below in conjunction with FIG. 10, to increment its ...

11/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00316195
High speed image processing computer employing video drams to produce raster scan pixel data.
Hochgeschwindigkeitsbildverarbeitungsrechner mit Videodynamischen Speichern mit wahlfreiem Zugriff zur Erzeugung von Rasterbildelementen.
Calculateur de traitement d'image a grande vitesse utilisant des memoires video dynamiques a acces aleatoire pour produire des elements d'image par balayage tra
PATENT ASSIGNEE:
VISUAL INFORMATION TECHNOLOGIES, INC., (1015100), 3460 Lotus, Plano Texas 75075, (US), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Pfeiffer, David Michael, 913 Baxter, Plano Texas 75023, (US)
Stoner, David Thornton, 16185 Red Oak Circle, McKinney Texas 75069, (US)
Thompson, Jay Allison, 6500 Palmer Trail, Plano Texas 75023, (US)
Miller, John B., 804 Whitehall, Plano Texas 75023, (US)
LEGAL REPRESENTATIVE:

Howick, Nicholas Keith et al (45951), CARPMAELS & RANSFORD 43 Bloomsbury Square, London WC1A 2RA, (GB)
PATENT (CC, No, Kind, Date): EP 308125 A2 890322 (Basic)
EP 308125 A3 910320
APPLICATION (CC, No, Date): EP 88308253 880907;
PRIORITY (CC, No, Date): US 96933 870914
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: G09G-001/16; G06F-015/66;
ABSTRACT WORD COUNT: 245

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	412
SPEC A	(English)	EPABF1	47595
Total word count - document A			48007
Total word count - document B			0
Total word count - documents A + B			48007

...SPECIFICATION can be used to generate a 64-bit wide write mask. A great deal of flexibility is thereby provided for masking certain bits of the **numerous pixels** . While **pixel** write mask information could be generated within the **parallel** image **processor** set 72, in the preferred embodiment of the invention, the image algorithm processor 66 generates such write mask information. Those skilled in the art may find it expedient in other situations to generate memory write mask information utilizing a **flag** register or less significant bit information of each of the 8-bit pixels carried on the internal 64-bit bus (C-BUS) throughout the **parallel** image **processor** set 72. In any event, the mask/**flag** bus 85 carries information which is expanded into a 64-bit word during the write mask cycles of the image memory 82.

As noted above...The concurrent operation of such address and data processing circuits enable high-speed access to the image memory. The image memory and the pixel data **processors** are constructed to **simultaneously process plural** words of **pixel** data. Thus, not only is high-speed image data **processing** made possible, but also the **parallel processing** of **plural** words of **pixel** data. The image memory of the invention utilizes video DRAMS to permit independent operation of the dynamic random access portion thereof for pixel data processing purposes, as well as a serial **shift register** portion thereof for temporary pixel data storage for serial transferral to the video output section. By utilizing a large number of such video DRAMs, a ...

video DRAMS

...includes a red, green and blue planes, each storing image color value data corresponding to the colors. Associated with each memory color plane is an **parallel** image **processor** and a video **processor** . Hence, pixel data for the primary colors is processed independently. The image memory further includes a viewable storage area which is much larger than that ...

11/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00316193
High speed image processing computer.
Hochgeschwindigkeitsbildverarbeitungsrechner.
Calculateur de traitement d'image a grande vitesse.
PATENT ASSIGNEE:
VISUAL INFORMATION TECHNOLOGIES, INC., (1015100), 3460 Lotus, Plano Texas 75075, (US), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Pfeiffer, David Michael, 913 Baxter, Plano Texas 75023, (US)
Stoner, David Thornton, 16185 Red Oak Circle, McKinney Texas 75069, (US)

Norsworthy, John Paul, 3638 Amanda Circle, Carrollton Texas 75007, (US)
Dipert, Dwight David, 2039 Cap Rock Drive, Richardson Texas 75080, (US)
Thompson, Jay Allison, 6500 Palmer Trail, Plano Texas 75023, (US)
Fontain, James Andrew, 737 Warwick Drive, Plano Texas 75023, (US)
Corry, Michael Kenneth, 4061 Port Royal, Dallas Texas 75244, (US)
LEGAL REPRESENTATIVE:
Howick, Nicholas Keith et al (45951), CARPMAELS & RANSFORD 43 Bloomsbury Square, London WC1A 2RA, (GB)
PATENT (CC, No, Kind, Date): EP 308124 A2 890322 (Basic)
EP 308124 A3 910206
APPLICATION (CC, No, Date): EP 88308251 880907;
PRIORITY (CC, No, Date): US 97664 870914
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: G06F-015/66; G09G-001/16;
ABSTRACT WORD COUNT: 196

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1655
SPEC A	(English)	EPABF1	47612
Total word count - document A			49267
Total word count - document B			0
Total word count - documents A + B			49267

...SPECIFICATION can be used to generate a 64-bit wide write mask. A great deal of flexibility is thereby provided for masking certain bits of the **numerous pixels** . While **pixel** write mask information could be generated within the **parallel** image **processor** set 72, in the preferred embodiment of the invention, the image algorithm processor 66 generates such write mask information. Those skilled in the art may find it expedient in other situations to generate memory write mask information utilizing a **flag** register or less significant bit information of each of the 8-bit pixels carried on the internal 64-bit bus (C-BUS) throughout the **parallel** image **processor** set 72. In any event, the mask/**flag** bus 85 carries information which is expanded into a 64-bit word during the write mask cycles of the image memory 82.
As noted above...The concurrent operation of such address and data processing circuits enable high-speed access to the image memory. The image memory and the pixel data **processors** are constructed to **simultaneously process plural** words of **pixel** data. Thus, not only is high-speed image data **processing** made possible, but also the **parallel processing** of **plural** words of **pixel** data. The image memory of the invention utilizes video DRAMS to permit independent operation of the dynamic random access portion thereof for pixel data processing purposes, as well as a serial **shift register** portion thereof for temporary pixel data storage for serial transferral to the video output section. By utilizing a large number of such video DRAMs, a ...

...includes a red, green and blue planes, each storing image color value data corresponding to the colors. Associated with each memory color plane is an **parallel** image **processor** and a video **processor** . Hence, pixel data for the primary colors is processed independently. The image memory further includes a viewable storage area which is much larger than that ...

11/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00197230
Method for emphasizing sharpness in a picture signal reproducing machine.
Verfahren zur Verstarkung der Scharfe in einer Maschine zur Wiedergabe eines Bildsignals.
Procede pour renforcer la nettete dans une machine de reproduction d'un

signal d'image.
PATENT ASSIGNEE:
Dainippon Screen Mfg. Co., Ltd., (507661), 1-1, Tenjinkitamachi Teranouchi-Agaru 4-chome Horikawa-Dori, Kamikyo-ku Kyoto 602, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Tomohisa, Kunio, 13, Nakaadachi-cho Yoshida, Sakyo-ku Kyoto, (JP)
Cho, Masamichi Room 202, Kopo Morita 32, Minami Takagamine-cho Takagamine Kita-ku, Kyoto-shi Kyoto-fu, (JP)
Kurusu, Yasuo, 14-2, Kitageni-cho Koyama, Kita-ku Kyoto, (JP)
LEGAL REPRESENTATIVE:
Haft, Berngruber, Czybulka (100851), Postfach 14 02 46 Hans-Sachs-Strasse 5, W-8000 Munchen 5, (DE)
PATENT (CC, No, Kind, Date): EP 198161 A1 861022 (Basic)
EP 198161 B1 910814
APPLICATION (CC, No, Date): EP 86101455 860205;
PRIORITY (CC, No, Date): JP 8571132 850405
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H04N-001/40; G03F-003/08;
ABSTRACT WORD COUNT: 110

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	589
CLAIMS B	(German)	EPBBF1	550
CLAIMS B	(French)	EPBBF1	692
SPEC B	(English)	EPBBF1	5197
Total word count - document A			0
Total word count - document B			7028
Total word count - documents A + B			7028

...SPECIFICATION the main scanning direction, and from the main scanning line memory 31 all signals on identical main scanning positions of each of the lines are **simultaneously** read out. These signals are **processed simultaneously** by a main scanning sequence arranging circuit 32, a weighting means 36, an adding means 33 and a dividing means 37, and from density information of a **plurality** of **pixels** arranged in the sub-scanning direction, picture signals (U(sub(y))) which are vignetted in the same direction are output. The picture signals (U(sub(y))) vignetted in the sub-scanning direction are input to a **shift register** 41 having a constant number of stages in the unsharp mask processing circuit 4 in the main scanning direction.

The shift register 41 outputs its...converter 2 input to the line memory 31 in the main scanning direction of the sub-scanning unsharp mask processing circuit 3. The unsharp mask **processing** circuit 3 **simultaneously processes** picture signals of shares of a plurality of scanning lines in the main scanning direction through the sub-scanning priority (sequence) aligning circuit 32 and a mask filter circuit 331, and outputs the vignette picture signal (U(sub(y))(ij)) from density information of a **plurality** of **pixels** aligning in the sub-scanning direction. The vignette picture signal (U(sub(y))(ij)) in the sub-scanning direction is input to the **shift register** 41 of appropriate stages in the unsharp mask processing circuit 4 in the main scanning direction.

The shift register 41 outputs its contents in each...

11/3,K/7 (Item 1 from file: 349)
DIALOG(R)File 349:PCT Fulltext

00579707 **Image available**
MULTIPLE MODE DIGITAL X-RAY IMAGING SYSTEM
SYSTEME D'IMAGERIE NUMERIQUE AUX RAYONS X A MODES MULTIPLES
Patent Applicant/Assignee:
VARIAN ASSOCIATES INC, VARIAN ASSOCIATES, INC. , 3050 Hansen Way, Palo

Alto, CA 94304 , US
Inventor(s):
COLBETH Richard E, COLBETH, Richard, E. , 1243 Richardson Avenue, Los Altos, CA 94024 , US
PAVOKOVICH John M, PAVOKOVICH, John, M. , 2945 Alexis Drive, Palo Alto, CA 94304 , US
SEPPI Edward J, SEPPI, Edward, J. , 320 Dedalera Drive, Portola Valley, CA 94028 , US
SHAPIRO Edward G, SHAPIRO, Edward, G. , 252 Andsbury Avenue, Mountain View, CA 94043 , US
Patent and Priority Information (Country, Number, Date):
Patent: WO 9824059 A1 19980604
Application: WO 97US21685 19971126 (PCT/WO US9721685)
Priority Application: US 96753799 19961129; US 9656926 19961129; US 97978177 19971125
Designated States: AU CA JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Filing Language: English
Fulltext Word Count: 14816

Fulltext Availability:
Detailed Description

Detailed Description
... ones or multiple adjacent ones of the first group of columns of super pixels, respectively.

In accordance with another aspect of the present invention, data **flags** are used to identify defective pixels within the detector array and are inserted into the data stream collected from the detector array for dynamic processing...defective pixels individually or in groups includes a data processing circuit and a data selection circuit. The data processing circuit is configured to receive and **process together** a plurality of successive sets of image data with a corresponding plurality of successive sets of correction data and in accordance therewith provide a plurality of successive sets of corrected image data. The plurality of successive sets of image data represents a **plurality** of **pixels** corresponding to a two-dimensional image, the plurality of successive sets of correction data represents a plurality of correction factors, each one of the plurality of correction factors corresponds to a respective one of the **plurality** of **pixels** and each one of the plurality of successive sets of correction data includes a data subset which indicates whether the respective one of the **plurality** of **pixels** is defective. The data selection circuit, coupled to the data processing circuit, is configured to receive and select between individual ones of the plurality of...

...a corresponding individual one of the plurality of successive sets of correction data when the data subset indicates that the corresponding respective one of the **plurality** of **pixels** is defective, and the individual one of the plurality of successive sets of selected data includes a corresponding one of the plurality of successive sets of corrected image data when the data subset does not indicate that the corresponding respective one of the **plurality** of **pixels** is defective.

In accordance with still another aspect of the present invention, a data buffer and filter is used to perform still image capture during...

11/3,K/8 (Item 2 from file: 349)
DIALOG(R)File 349:PCT Fulltext

00403083
SUBTITLING VIDEO DATA
DONNEES DE SOUS-TITRAGE VIDEO

Patent Applicant/Assignee:
SCREEN SUBTITLING SYSTEMS LTD
ATKINS David John
Inventor(s):
ATKINS David John
Patent and Priority Information (Country, Number, Date):
Patent: WO 9534165 A1 19951214
Application: WO 95GB1353 19950609 (PCT/WO GB9501353)
Priority Application: GB 9411615 19940609
Designated States: AM AT AU BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP LK LR LT LU LV MD MG MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TT UA VN KE MW SD SZ UG AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 7172

Fulltext Availability:
Detailed Description

Detailed Description
... the word.

Runs of pixels are encoded resulting in codes being transferred to the output buffer 703. The analysing logic 706 is aware of how **many pixels** have been coded from the input stream, therefore this logic allows an appropriate number of contiguous input pixels to be supplied to the **shift register** 701. In this way, run-length encoding is optimised so as to reduce the requirement on transition bandwidth. Thus, by using the look-up table...

...a recursive loop, as illustrated in Figure 7, it is possible to optimise run-length encoding and thereby optimise transitional storage bandwidth, while at the **same time** substantially increasing **processing** speed by considering a **plurality** of input **pixel** values in parallel. Furthermore, given this level of optimisation, it is not necessary to adapt values stored within the look-up table 702, therefore it...

18/5/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01177015
Image processing
Bildverarbeitung
Traitement d'images
PATENT ASSIGNEE:
SONY CORPORATION, (214025), 6-7-35 Kitashinagawa Shinagawa-ku, Tokyo 141, (JP), (Applicant designated States: all)
INVENTOR:
Kurose, Yoshikazu, c/o Sony Corporation , 6-7-35 Kitashinagawa, Shinagawa-ku, Tokyo 141, (JP
LEGAL REPRESENTATIVE:
Pratt, Richard Wilson et al (46458), D. Young & Co, 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 1026636 A2 000809 (Basic)
APPLICATION (CC, No, Date): EP 300677 000128;
PRIORITY (CC, No, Date): JP 9929020 990205
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06T-015/00
ABSTRACT EP 1026636 A2
An image processing apparatus can perform a variety of graphic processing using a video signal obtained by an image pickup apparatus. The apparatus comprises a DDA set-up circuit (10) for generating first image data and first z-data, a triangle circuit (11), a texture engine circuit (12), and a memory interface circuit (13) for writing the first image data and the first z-data respectively in a display buffer memory (21) and a z-buffer memory (22) and for writing the second image data and the second z-data respectively to the display buffer memory and the z-buffer memory when second image data corresponding to image pickup results of an image pickup apparatus and second z-data corresponding to the second image data are input from the video signal generator (30).
ABSTRACT WORD COUNT: 127
NOTE:
Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 000809 A2 Published application without search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200032	1116
SPEC A	(English)	200032	6274
Total word count - document A			7390
Total word count - document B			0
Total word count - documents A + B			7390

18/5/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00439210
Digital data transmission system having error detecting and correcting function
Digitales Datenubertragungssystem mit Fehlererkennung und Fehlerkorrektur
Systeme de transmission de donnees numeriques avec detection et correction d'erreur
PATENT ASSIGNEE:
SONY CORPORATION, (214021), 7-35 Kitashinagawa 6-chome Shinagawa-ku, Tokyo 141, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Suzuki, Hideto, c/o Sony Corporation, 7-35 Kitashinagawa 6-chome,

Shinagawa-ku, Tokyo, (JP)
Kurose, Yoshikazu , c/o Sony Corporation, 7-35 Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
Aoki, Shinji, c/o Sony Corporation, 7-35 Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP
LEGAL REPRESENTATIVE:
Thevenet, Jean-Bruno et al (39781), Cabinet Beau de Lomenie 158, rue de l'Universite, 75340 Paris Cedex 07, (FR)
PATENT (CC, No, Kind, Date): EP 415853 A2 910306 (Basic)
EP 415853 A3 930728
EP 415853 B1 971119
APPLICATION (CC, No, Date): EP 90402414 900831;
PRIORITY (CC, No, Date): JP 89225855 890831
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G11B-020/14; G11B-020/18; H03M-013/00;
CITED PATENTS (EP A): GB 2201067 A
CITED REFERENCES (EP A):
PATENT ABSTRACTS OF JAPAN vol. 9, no. 113 (P-356)17 May 1985
PATENT ABSTRACTS OF JAPAN vol. 10, no. 113 (E-399)26 April 1986;

ABSTRACT EP 415853 A2
An error correction code of the product sign format is added to the input information data to form coded data. The coded data are then NRZI converted and recorded onto a record medium together with identification data of a predetermined data pattern. Error detecting and correcting processing is executed with reproduction data obtained from the record medium to reproduce the data recorded on the record medium. The device comprises an NRZI converting circuit for outputting the information data as they are without NRZI converting the same but for NRZI converting the coded data using the last bit of the identification data as an initial value, and a memory controlling circuit (501) for controlling writing and reading of a memory, which is provided to convert the reproduction data from a series of inner codes into another series of outer codes, so that write address information for the memory which is obtained from the reproduction data may be compensated for when it is not obtained properly and outer code error detecting and correcting processing may be executed in a trouble-free way. (see image in original document)
ABSTRACT WORD COUNT: 188

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	910306	A2	Published application (Alwith Search Report ;A2without Search Report)
Change:	930714	A2	Obligatory supplementary classification (change)
Search Report:	930728	A3	Separate publication of the European or International search report
Examination:	940309	A2	Date of filing of request for examination: 940105
Examination:	951213	A2	Date of despatch of first examination report: 951031
Grant:	971119	B1	Granted patent
Oppn None:	981111	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9711W2	1857
CLAIMS B	(German)	9711W2	1391
CLAIMS B	(French)	9711W2	2146
SPEC B	(English)	9711W2	11754
Total word count - document A			0
Total word count - document B			17148
Total word count - documents A + B			17148

18/5/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00432188
Information transmitting device.
Informationsubertragungsgerat.
Dispositif pour la transmission d'informations.
PATENT ASSIGNEE:
SONY CORPORATION, (214022), 7-35, Kitashinagawa 6-chome Shinagawa-ku, Tokyo, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Kurose, Yoshikazu , c/o Sony corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
Aoki, Shinji, c/o Sony corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
Suzuki, Hideto, c/o Sony corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP
LEGAL REPRESENTATIVE:
Ayers, Martyn Lewis Stanley et al (42851), J.A. KEMP & CO. 14 South Square Gray's Inn, London WC1R 5LX, (GB)
PATENT (CC, No, Kind, Date): EP 410722 A2 910130 (Basic)
EP 410722 A3 940126
APPLICATION (CC, No, Date): EP 90308148 900725;
PRIORITY (CC, No, Date): JP 89194769 890726
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G11B-027/30; G11B-020/12; G11B-020/18; H04L-001/00;
CITED PATENTS (EP A): EP 146636 A; EP 245874 A; EP 323890 A; EP 203592 A; GB 2075792 A; EP 242093 A
CITED REFERENCES (EP A):
PATENT ABSTRACTS OF JAPAN vol. 9, no. 177 (P-375)(1900) 23 July 1985 & JP-A-60 050 665 (HITACHI SEISAKUSHO K.K.) 20 March 1985;

ABSTRACT EP 410722 A2
In an information transmitting device which transmits information on a preamble portion and a plurality of data blocks as one unitary set, when a block synchronising code in the data blocks is detected, the timing of the detection and the block synchronising code determined correct or subject to error correction are utilised to reproduce information contained in the preamble portion. The device is applicable, but not limited, to information recorded in a helical scan VTR format. (see image in original document)
ABSTRACT WORD COUNT: 83

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	910130 A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	940126 A3	Separate publication of the European or International search report
Change:	940713 A2	Representative (change)
Examination:	940831 A2	Date of filing of request for examination: 940704
Examination:	950830 A2	Date of despatch of first examination report: 950714
Withdrawal:	971112 A2	Date on which the European patent application was deemed to be withdrawn: 970521

LANGUAGE (Publication,Procedural,Application): English; English; English

18/5/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00420442
Digital data transmitting apparatus
Gerat zur Ubertragung von digitalen Daten
Appareil de transmission de donnees numeriques
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PATENT (CC, No, Kind, Date): EP 418885 A2 910327 (Basic)
EP 418885 A3 940216
EP 418885 B1 970416
APPLICATION (CC, No, Date): EP 90118117 900920;
PRIORITY (CC, No, Date): JP 89244468 890920
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H04L-007/08;
CITED PATENTS (EP A): EP 269974 A; EP 133081 A; EP 236017 A

ABSTRACT EP 418885 A2
An apparatus for transmitting digital data inclusive of information data and synchronous data having a plural-byte code inserted per predetermined byte length of the information data. The apparatus comprises a sync code position predictive means (41, 45) for predicting the top position of the sync code by converting the transmission digital data into parallel data at a desired timing and then comparing each byte of the parallel data with a desired byte of the sync code; and a sync code detection means (44, 46) for detecting the sync code in the transmission digital data by first extracting the parallel data by a length corresponding to the plurality of bytes of the sync code in accordance with the result of such prediction of the sync code position predictive means (41, 45), and then comparing the extracted parallel data with the sync code. (see image in original document)
ABSTRACT WORD COUNT: 148

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	910327	A2	Published application (A1with Search Report ;A2without Search Report)
Change:	930512	A2	Representative (change)
Change:	940202	A2	Obligatory supplementary classification (change)
Search Report:	940216	A3	Separate publication of the European or International search report
Examination:	940921	A2	Date of filing of request for examination: 940721
Examination:	950510	A2	Date of despatch of first examination report: 950322
Grant:	970416	B1	Granted patent
Oppn None:	980408	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	163
CLAIMS B	(English)	EPAB97	260
CLAIMS B	(German)	EPAB97	236
CLAIMS B	(French)	EPAB97	288
SPEC A	(English)	EPABF1	7567
SPEC B	(English)	EPAB97	7090
Total word count - document A			7730
Total word count - document B			7874
Total word count - documents A + B			15604

18/5/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00363525

Sampling frequency converter

Abtastfrequenz-Konverter

Convertisseur de frequence d'echantillonnage

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PATENT (CC, No, Kind, Date): EP 336669 A2 891011 (Basic)
EP 336669 A3 901128
EP 336669 A3 901212
EP 336669 B1 961009

APPLICATION (CC, No, Date): EP 89303242 890403;

PRIORITY (CC, No, Date): JP 8886678 880408

DESIGNATED STATES: DE; FR; GB; NL

INTERNATIONAL PATENT CLASS: H03H-017/06;

CITED PATENTS (EP A): US 4460890 A; EP 262647 A; FR 2582893 A; EP 80712 A; US 4558348 A

ABSTRACT EP 336669 A2

A sampling frequency converter of a simplified constitution for use in a format conversion apparatus designed to convert sampled input data (2, 4) of an input sampling frequency into sampled output data of an output sampling frequency. The converter comprises over-sampling means (13) supplied with the sampled input data for increasing the sampling frequency of the sampled input data by a predetermined factor or coefficient to provide over-sampled data; an output data extractor (14, 15) for periodically extracting data from the over-sampled data in response to a timing pulse having the output sampling frequency; and a controller (11) for controlling the phase of the timing pulse to control the phase of the sampled output data. One of the sampled input and output data is a digital color signal such as a luminance signal conforming with the digital composite color signal format, while another of the sampled input and output data is a digital color signal such as a luminance signal conforming with the digital component signal format. And the controller serves to control the phase of the timing pulse in such a manner that the group delay imparted to the digital luminance signal becomes equal to the delay imparted to the digital color signal.

ABSTRACT WORD COUNT: 208

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	891011	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	901128	A3	Separate publication of the European or International search report
*Search Report:	901205	A2	Separate publication of European or Intl search report (change)
Search Report:	901212	A3	Separate publication of the European or International search report
Examination:	910731	A2	Date of filing of request for examination: 910531
Examination:	940202	A2	Date of despatch of first examination report: 931220

Grant: 961009 B1 Granted patent
Oppn. None: 971001 B1 No opposition filed
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	386
CLAIMS B	(English)	EPAB96	473
CLAIMS B	(German)	EPAB96	424
CLAIMS B	(French)	EPAB96	570
SPEC A	(English)	EPABF1	6175
SPEC B	(English)	EPAB96	6117
Total word count - document A			6561
Total word count - document B			7584
Total word count - documents A + B			14145